System-On-Chip Technologies

Specification Sheet

H.264-to-MPEG2 Transcoder IP Core

Product Description

SOC provides the H.264-to-MPEG2 transcoder in both FPGA IP core format and a standalone all-in-one modules.

IP cores are available for both Xilinx and Altera FPGAs. The input and output for the transcoder can be in either elementary or TS stream format.

The SOC H.264-to-MPEG2 transcoder module is a System-on-Module (SoM) card that can be connected to a user device/PCB using a standard DDR3 memory connector. It can interface with an FPGA or a microprocessor for user product integration or connect to I/O interface chips for direct product design and fabrication.

SOC also offers product development boards, which allow users to develop products using the SOC codec IP cores or modules.

Users have the options of using the codec modules or licensing SOC IP cores for production after prototyping.

Key Features

- All-hardware
- High Speed (Low latency)
- Small Silicon Footprint
- Low Power
- High Reliability (due to hardware architecture)
- High transcoding accuracy
- Automatic adapting profiles
- Up to 60fps
- User controllable API
- Option of IP Core or Module
- Video Transmission (Network) Cores available
- Development Board available

Specifications

- Standard: H.264 and MPEG-2 (ISO/IEC14496-10 and ISO/IEC 13818)
- Profiles: High, Main, Baseline
- Video resolutions: Up to 1080i/p
- Frame Rate: Up to 60fps
- Chroma Formats: 4:2:2 or 4:2:0
- Input format: H.264 Elementary, or Transport Stream
- Output format: MPEG-2 Elementary, or Transport Stream
- Latency: 0.5ms
- Power Consumption: 1.5w (IP core)

FPGA Resources

- **Xilinx FPGAs**
  Spartan-6 LX150
  Artix-7 A200T, 2 channels
  Kintex-7 K325, 4 channels

- **Altera FPGAs**
  Cyclone-IV, V
  Arria-V
  Stratix-IV, V.

H.264-to-MPEG2 Transcoder Module

H.264 Compressed Video/Audio Stream

Support multiple channels

MPEG-2 Compressed Video/Audio Stream

Temperature Range: $0 – 75^0$ C and $-40^0 – +80^0$

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