SOC Module ID

API Specification

Introduction

The API interface has 256 register (16 bit for writing and 32 bits for reading). Each register has an address to allow user-access. The registers accept command code for controlling the operation of the features within the FPGA. The registers may be read to acquire status and debugging information.

Some registers are allocated for user configurations and the rest are reserved for system functions such as debugging. The following table(s) specifies the address, definition, and access right (read/write) for the user-accessible registers. Note: registers of any API_TYPE that are NOT in the table are not designed for user access. If such a register is written to, the decoder may stop running. To recover, the core must be re-downloaded into the FPGA.

Control the API inside the FPGA

If it is necessary to control the API via the modules inside the FPGA, the ports of the API are available. Details, including the clock frequency, are provided in the corresponding integration manual.

Control the API outside the FPGA

If it is necessary to control the Decoder from outside the FPGA, the address, date, and R/W pins can be routed to the FPGA I/O pins. The desired FPGA I/O pins for the API may be selected or the SOC default pins may be used. An UART interface is available, upon request. The interface provides access to the API via uart_tx and uart_rx pins.

Table-1: General Core Registers

Addr (HEX)	Information	Access
FC	Bit[31]: Board Type - 0=Carrier Board - 1=Module Bit[27:24]: Image Type - 0= Golden - 1 = Update Bit[23:20]: Board Type (optional) - 0 = VTR Encoder - 1 = VTR Decoder - 3 = VTRS Decoder - 8 = VTR Encoder with HDMI option Bit[15:8]: Version – Major Rev Bit[7:0]: Version – Minor Rev	R

