SOC VoIP-X-4K Network API Specification

Revision History

The following table shows the revision history for this document.

Date (MM/DD/YYYY)	Version	Notes
06/24/2020	1.0	SOC initial Release

Introduction

The API interface has 256 register (16 bit for writing and 32 bits for reading). Each register has an address to allow user-access. The registers accept command code for controlling the operation of the features within the FPGA. The registers may be read to acquire status and debugging information.

Some registers are allocated for user configurations and the rest are reserved for system functions such as debugging. The following table(s) specifies the address, definition, and access right (read/write) for the user-accessible registers. Note: registers of any API_TYPE that are NOT in the table are not designed for user access. If such a register is written to, the decoder may stop running. To recover, the core must be re-downloaded into the FPGA.

Control the API inside the FPGA

If it is necessary to control the API via the modules inside the FPGA, the ports of the API are available. Details, including the clock frequency, are provided in the corresponding integration manual.

Control the API outside the FPGA

If it is necessary to control the CODEC from outside the FPGA, the address, date, and R/W pins can be routed to the FPGA I/O pins. The desired FPGA I/O pins for the API may be selected or the SOC default pins may be used. An UART interface is available, upon request. The interface provides access to the API via UART_RX and UART_TX pins.

SOC Network status and control registers

(w) : writable bit(s)
(t) : toggle write bit(s) – write '1' to toggle bit value

Note: Any register bit not listed is reserved for internal use only. All register bits are read-only unless marked with (w) or (t).

<table>
<tr><th>Addr (hex)</th><th>Information</th><th>Default (hex)</th><th>Access</th></tr>
<tr><td>A0</td><td>TX Target IP address is divided into 4 bytes (see example in the table below)

Read:
Bit[31:0]: TX Target IP address [31:0] (Byte 3 ~ Byte 0)

Write:
Bit[9:8](w): TX Target IP address byte index (3~0)
Bit[7:0](w): TX Target IP address byte

<table>
<tr><td>Target IP Address</td><td colspan="4">192.168.1.101</td></tr>
<tr><td>Byte index</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Target IP byte</td><td>C0</td><td>A8</td><td>01</td><td>65</td></tr>
</table>
</td><td>Encoder:
C0A80165
Decoder:
C0A80164</td><td>R/W</td></tr>
<tr><td>A1</td><td>Reserved</td><td>00000000</td><td>RO</td></tr>
<tr><td>A2</td><td>Reserved</td><td>00000001</td><td>R/W</td></tr>
<tr><td>A3</td><td>Reserved</td><td>00000000</td><td>RO</td></tr>
<tr><td>A4</td><td>Bit[15:0](w): TX Target UDP Port.</td><td>000004D2</td><td>R/W</td></tr>
<tr><td>A5</td><td>Bit[15:0](w): TX Packet Size (Bytes)</td><td>00000578</td><td>R/W</td></tr>
</table>

<table>
<tr><th>Addr (hex)</th><th>Information</th><th>Default (hex)</th><th>Access</th></tr>
<tr><td>A6</td><td>MAC address is divided into 6 bytes (see example in the table below)

Read:
Bit[31:0]: MAC address[31:0] (Byte 3 ~ Byte 0)

Write:
Bit[10:8](w): MAC address byte index (5~0)
Bit[7:0](w): MAC address byte
A Network Soft Reset is required for MAC address change (See Addr 0xAF)

<table>
<tr><td>MAC Address</td><td colspan="6">BA : 98 : 76 : 54 : 32 : 10</td></tr>
<tr><td>Byte index</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>MAC byte</td><td>BA</td><td>98</td><td>76</td><td>54</td><td>32</td><td>10</td></tr>
</table>
</td><td>Vary by board</td><td>R/W</td></tr>
<tr><td>A7</td><td>Bit[31:16]: MAC address[47:32] (Byte 5 ~ Byte 4)
Bit[15:14](w): Number of packets buffered in Network Stack minus 1.
Bit[13:0](w): Inter-packet Delay (unit: cycles of network TX clock).</td><td>1Gbps:
XXXX05DC
100Mbps:
XXXX0064</td><td>R/W</td></tr>
</table>

<table>
<tr><th>Addr (hex)</th><th>Information</th><th>Default (hex)</th><th>Access</th></tr>
<tr><td>A8</td><td>Gateway IP address is divided into 4 bytes (see example in the table below)

Read:
Bit[31:0]: Gateway IP address [31:0] (Byte 3 ~ Byte 0)

Write:
Bit[9:8](w): Gateway IP address byte index (3~0)
Bit[7:0](w): Gateway IP address byte
Set to 0 if using automatic gateway from DHCP.
A Network Soft Reset is required for any Gateway change (See Addr 0xAF).

<table><tr><td>Gateway IP Address</td><td colspan="4">192.168.1.1</td></tr><tr><td>Byte index</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Target IP byte</td><td>C0</td><td>A8</td><td>01</td><td>01</td></tr></table></td><td>00000000</td><td>R/W</td></tr>
<tr><td>A9</td><td>Reserved</td><td>00000000</td><td>RO</td></tr>
<tr><td>AA</td><td>Board IP address is divided into 4 bytes (see example in the table below)

Read:
Bit[31:0]: Board IP address [31:0] (Byte 3 ~ Byte 0)

Write:
Bit[9:8](w): Board IP address byte index (3~0)
Bit[7:0](w): Board IP address byte

<table><tr><td>Target IP Address</td><td colspan="4">192.168.1.100</td></tr><tr><td>Byte index</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Target IP byte</td><td>C0</td><td>A8</td><td>01</td><td>64</td></tr></table></td><td>Encoder:
C0A80164
Decoder:
C0A80165</td><td>R/W</td></tr>
</table>

Addr (hex)	Information	Default (hex)	Access
AB	Reserved	00000000	RO
AC	Reserved	00000000	RO
AD	Bit[15:0](w): RX UDP Port	000004D2	RW
AE	Bit[0](w):Check TX packet format for Transport Stream compliance. If set to '1', only Transport Stream packets will be sent out.	00000001	R/W
AF	Bit[3](t): Bypass DHCP (Toggle Write) - 0: Obtain an IP from DHCP server - 1: Bypass DHCP and use the default IP Bit[2](t): Static IP Enable (Toggle Write) - 0: Only assign IP address on successful DHCP handshake - 1: Use static board IP address set in registers 0xAA~0xAD if DHCP fails Bit[1]: Network Speed - 0: 100Mbps - 1: 1Gbps Bit[0](w): Network Soft Reset (Self-clear)	1Gbps: 00000006 100Mbps: 00000004	R/W