SOC Generic Decoder System

API Specification

Revision: 1.3
2017.4.26

Revision History

The following table shows the revision history for this document.

Date	Comment	Revision	Author
	Old versions	1.0	
2016.10.24	Added register BF to the API manual.	1.1	Blake
2016.12.20	Audio PID selectable (0x92)	1.2	Chad
2017.04.26	Add DDR calib register(0x40)	1.3	Blake

Introduction

The API interface has 256 register (16 bit for writing and 32 bits for reading). Each register has an address to allow user-access. The registers accept command code for controlling the operation of the features within the FPGA. The registers may be read to acquire status and debugging information.

Some registers are allocated for user configurations and the rest are reserved for system functions such as debugging. The following table(s) specifies the address, definition, and access right (read/write) for the user-accessible registers. Note: registers of any API_TYPE that are NOT in the table are not designed for user access. If such a register is written to, the decoder may stop running. To recover, the core must be re-downloaded into the FPGA.

Control the API inside the FPGA

If it is necessary to control the API via the modules inside the FPGA, the ports of the API are available. Details, including the clock frequency, are provided in the corresponding integration manual.

Control the API outside the FPGA

If it is necessary to control the Decoder from outside the FPGA, the address, date, and R/W pins can be routed to the FPGA I/O pins. The desired FPGA I/O pins for the API may be selected or the SOC default pins may be used. An UART interface is available, upon request. The interface provides access to the API via uart_tx and uart_rx pins.

Table-1: General Core Registers

Addr (HEX)	Information	Access

40	Read only (**DO NOT** write to this register): Bit [2]: DDR_CALIB_OK. '1' = DDR calibration ok. '0' = DDR calibration failed, please check your DDR type and connections.	**R**
90	Bit[31:0]: PTS-PCR Difference From Transport Stream	R
91	Bit[31:0]: Transport Stream ID Select	R/W
92	**Writing:** Bit[15]: - 0 = Set Video PID - 1 = Set Audio PID Bit[12:0]: Transport Stream PID **Reading:** Bit[28:16]: Audio 1 PID Bit[12:0]: Video 1 PID	R/W
93	Bit[12:0]: Transport Video Stream 2 PID	R/W
94	Bit[12:0]: Transport Video Stream 3 PID	R/W
95	Bit[12:0]: Transport Video Stream 4 PID	R/W
9B	Bit[0]: Reset AV Sync Module	R/W
9C	Bit[1]: Override Interlaced Enable Bit[0]: Override Interlaced Mode	R/W
9D	Bit[3]: Override Frame Rate Enable Bit[2:0]: Frame Rate Mode - "111" = 60Hz - "101" = 50 Hz - "100" = 30 Hz - "010" = 25 Hz - "001" = 24 Hz	R/W
9F	Bit[2:0]: Override Video Display Resolution - "000" = Use Stream Resolution - "001" = 720x480 - "010" = 1280x720 - "011" = 1920x1080 - "100" = 720x576 - "101" = 640x480	R/W
B0	Bit[5:0]: Override Display Frame Position	R/W

	- Only used when 0xB1=2	
B1	Bit[1:0]: Override Display Frame Mode - "00" = Normal A/V Sync - "01" = Display Last Decoded - "10" = Display Frame reference by register 0xB0 - "11" = Display current Decoding Frame	
B3	Bit[12]: Enable Auto Low Delay mode. (May not be compatible with all TS stream). This function will auto adjust the video presentation time to the lowest possible. Bit[11]: Truncate active video range for compliance with TRS embedded video codes. Bit[10]: Allow expired frame to be display if newer than current displayed frame Bit[8]: Debug Overlay Enable	R/W
B4	Bit[4]: TS MPEG2 Stream Detected Bit[3]: TS H264 Stream Detected	R
B5	Bit[15:12]: TS Rx Sync Error Counter (user clock) Bit[11:8]: TS Rx Sync Error Counter (TS clock) Bit[7:4]: TS Rx Byte Count (TS clock) Bit[3:0]: TS Rx Byte Count (user clock)	R
B6	Bit[31:16]: TS Buffer Overflow Count Bit[15:0]: TS Demux Overflow Count	R
B7	Bit[1]: Bypass PCR Sync (PCR counter will free run) Bit[0]: New Stream Sync	R/W
B8	Bit[15:0]: PCR resync threshold. - PCR will only resync if difference is greater than the threshold. This allows the system to tolerate variable jitter	R/W

BF	Display timing threshold value (DTH): Bit [2:0]: DTH for progressive stream. The **unit** is a frame. Bit [10:8]: DTH for interlaced stream. The **unit** is the first field, typically the top field. *This register is to control latency for progressive and interlaced scenario, respectively. DTH =0: The frame is submitted to display only when the whole (100%) **unit** is received and decoded. **This is the default and most safe value.** DTH =1 to 7: The frame is submitted to display when DTH x12.5 % of the **unit** is received and decoded. ******Important notes:*** *Be careful to use this register with a low value. Due to the input stream is possibly not constant coming, the low value (for*	R/W
	example DTH =*2 for only 25%) could cause the display jitter or flashing. If this happen, the user should increase the* DTH.	
FC	Bit[31:0]: Decoder System Build Date	R
FD	Bit[31:0]: Decoder System Time Stamp	R
FE	Bit[11]: MPEG2 Core Present Bit[10]: H264 Core Present Bit[8]: PCM Buffer Present Bit[7]: DSP Interface Core Present Bit[5]: Video Output Core Present Bit[4]: Maximum 1080i Output Bit[3]: 50Hz minimum output frame rate Bit[2]: Watermark Present Bit[1]: FPGA DNA Authentication present Bit[0]: FPGA EEPROM Authentication present	R
FF	Bit[31:16]: Reset Count Bit[6]: Transport Stream Mode Bit[5]: Transport Stream Reset Bit[4]: Video Decoder Reset Bit[3]: Authentication Key OK Bit[2]: PTS Reset Enable* Bit[1]: Display Reset* Bit[0]: Decoder Reset*	R/W*

Table-2: Frame Sync API registers description

Addr (HEX)	Information	Access
70	Bit[31:16]: Output Expired Frame Counter Bit[15:0]: Output Frame Counter	R
71	Bit[15:0]: Input Invalid Frame Counter	R
72	Bit[15:0]: Input Expired Frame Counter	R
73	Bit[15:0]: PCR Clock Resync Counter	R
74	Bit[15:0]: Frames Duplicated	R
75	Bit[15:0]: Frames Skipped	R
76	Bit[1]: Trick Mode Running Bit[0]: Override Sync*	R/W*
77	Bit[5:0]: Buffer Frame Count	R
78	Bit[31:24]: Top Field Count Bit[23:16]: Bottom Field Count Bit[15:0]: Frame Count	R
7D	Bit[31:0]: Current Presentation Time	R
7E	Bit[31:0]: Last Displayed Presentation Time	W

Table-3: DDR Fifo Registers

The DDR fifo is a miniumum 8MB buffer to handle any incoming bandwidth spikes the BRAM is not sufficient for. In most application the DDR fifo will remain empty or below 10%.

Addr (HEX)	Information	Access
30	Bit[31:0]: Build Date	R

31	Bit[14]: Reset Bit[13]: Buffer Overflow Bit[10]: Byte Read Bit[9]: Output Buffer Empty Bit[8]: Output Buffer Ready Bit[3]: Timer Enabled* Bit[2]: Low Delay* Bit[1]: Clear Buffer Overflow Register* Bit[0]: API Reset*	R/W
32	Bit[5:0]: Burst Size Bit[8]: Bypass DDR Fifo (DDR will not be used)	R/W
33	Bit[25:0]: DDR Start Address	R
34	Bit[25:0]: DDR End Address	R
35	Bit[7:0]: DDR Buffer Percent	R
36	Bit[7:0]: DDR Buffer Count (Number of Blocks in DDR)	R
37	Bit[15:0]: Input Count	R
38	Bit[15:0]: Read Count	R

