SOC MPEG2 Decoder IP

API Specification

Introduction

The API interface has 256 register (16 bit for writing and 32 bits for reading). Each register has an address to allow user-access. The registers accept command code for controlling the operation of the features within the FPGA. The registers may be read to acquire status and debugging information.

Some registers are allocated for user configurations and the rest are reserved for system functions such as debugging. The following table(s) specifies the address, definition, and access right (read/write) for the user-accessible registers. Note: registers of any API_TYPE that are NOT in the table are not designed for user access. If such a register is written to, the decoder may stop running. To recover, the core must be re-downloaded into the FPGA.

Control the API inside the FPGA

If it is necessary to control the API via the modules inside the FPGA, the ports of the API are available. Details, including the clock frequency, are provided in the corresponding integration manual.

Control the API outside the FPGA

If it is necessary to control the Decoder from outside the FPGA, the address, date, and R/W pins can be routed to the FPGA I/O pins. The desired FPGA I/O pins for the API may be selected or the SOC default pins may be used. An UART interface is available, upon request. The interface provides access to the API via uart_tx and uart_rx pins.

Table-1 MPEG2 Core API registers description

Addr (HEX)	Information	Access
00	Bit[3]: Pipeline Reset Bit[2]: Stream Reset Bit[1]: Pause* Bit[0]: MPEG2 Core Reset*	R/W*
01	Bit[3]: Compression Type (0=MPEG2, 1= H264) Bit[2]: Chroma Format (0=4:2:0, 1=4:2:2) Bit[1]: Aspect Ratio (0=4:3, 1=16:9)	R
02	Bit[5:4]: Frame Format Bit[3:0]: Frame Rate	R
04	Bit[11:0]: Horizontal Resolution	R
06	Bit[11:0]: Vertical Resolution	R
07	Bit[7:0]: Profile IDC	R
08	Bit[7:0]: Level IDC	R
09	Bit[2]: Byte Stream Read Bit[1]: Byte buffer empty Bit[0]: Decoding	R

0A	Bit[6]: Decode Frame Enable Bit[5]: Decode Macroblock Enable Bit[4]: Wait for Pipeline Ready Bit[3]: Wait for Free Frame Location Bit[2]: Decoded Macroblock Buffer Ready Bit[1]: Temporal Macroblock Ready Bit[0]: Spatial Macroblock Ready	R
0E	Bit[31:0]: Decoded Frame Count	R
0F	Bit[31:0]: Decoding Error Count	
10	Bit[31:0]: Build Date	R
11	Bit[31:0]: Build Time	R
12	Bit[31:0]: Frame Error Count	R
13	Bit[6:4]: Current Frame Type Bit[2]: B Frame Present Bit[1]: P Frame Present Bit[0]: I Frame Present	R
14	Bit[4]: Quant Matrix Extension Present Bit[3]: 16x8 Motion Vector Present Bit[2]: Dual Prime Motion Vector Present Bit[1]: Frame Motion Vector Present Bit[0]: Field Motion Vector Present	R
24	Bit[31:0]: Bytes Read	R

