SOC Encoder System

API Specification

Version 2.3

Table-1: Encoder System Configuration

Addr (HEX)	Information	Access	Default
92	Bit[2:0]: Multi-Channel/Time Sharing API Core Selection - 0 – Selects all cores for writing - 1-7 = Core # - Note only 1 core can be read at a time. A value of 0 should not be used for reading registers. - This register is also used for indexing sub-API blocks such as Video Input, H264 Encoder	R/W	0x0000 0x0001
The following registers are unique to each time-shared core (when used)			
94	Bit[15:8]: Real-Time Encoding Frame Rate Bit[7:0]: Target Frame Rate	R	NA
96	Bit[15:0]: (Presentation Latency / 2.84ms) - Example: 0x1E = 85.2ms	R/W	0x0010
97	Bit[9:0]: Target Bit Rate Value / 10 (Mbps) - Example: 150(decimal) = 15Mbps	R/W	*0x0032
9E	The constant bitrate register is used to restrict the output rate to a specific duty cycle. Care must be taken to ensure the CBR is larger than the Target Bit Rate (0x97). Bit[14:0]: Constant Bitrate Value / 10 (Mbps) - Example: 150(decimal) = 15Mbps Bit[15]: Null TS Padding - When a **transport stream** is used the 'unused bandwidth' can be null-packet padded when this bit is enabled.	R/W	0x0000
The following registers are shared between all cores even when muli/time-sharing cores are used			
E5	Bit[31:16]: Codec Type: E265 = Encoder H265 Bit[15:0]: Firmware Version		
E6	Bit[31:0]: Build Date YYYYMMDD	R	NA
E7	Bit[31:0]: Build Time Stamp - ##HHMMSS	R	NA
9D	Bit[21]: Time limted Core Expired Bit[16]: Authentication Passed	R/W*	

	Bit[15]: EEPROM passed Bit[14]: DNA Passed Bit[13]: User TX Ready Bit[11]: Output Buffer Ready Bit[9]: DDR Fifo Buffer Present Bit[8]: EEPROM Authentication Present Bit[7]: DNA Authentication Present Bit[6]: Bypass Output DDR Fifo* Bit[3]: Disable CODEC Read* Bit[2]: Force CODEC Read* Bit[1]: Bypass Trsansport Stream DDR Fifo* Bit[0]: Bypass Transport Stream Encoder* Note: Bit with (*) is toggle bit, i,e. write '1' to this bit toggle the current value.		NA
9F	Bit[11:8]: Max encoding channel number Bit[3]: 4K encoding enabled Bit[2]: Audio enabled Bit[1]: FPS60 enabled Bit[0]: 10 bits encoding enabled	R	NA
E0	Bit[5]: Final Encoder Reset Bit[2]: WatchDog Reset Bit[1]: Enable WatchDog* (Wrtie x4321 to disable, x4320 to enable) Bit[0]: API Controlled Reset* (Write x55AA to trigger API reset)	R/W*	0x0012
E1	Bit[5:4]: Audio Select for Transport Stream The following Bits are toggle by writing '1' to the corresponding bit Bit[3]: Disable Video Bit[2]: Disable Audio	R/W	0x0010

*Default values with * may vary depending on customer request of initial value.*
Default values marked 'NA' have no default value as they are dependent on user content, vary by build (build date).

