MCM-1000A Encoder System

API Specification

Revision: 1.0
2016.06.20

Revision History

The following table shows the revision history for this document.

Date	Comment	Revision	Author
06/20/2016	Initial revision	1.0	Blake

Table-1: Encoder System Configuration

Addr (HEX)	Information	Access
A1	Bit[3:0]: Audio encoder selection * 0xA: MPEG2 layer 2, 96Kbps 0xB: MPEG2 layer 2, 160Kbps 0xC: MPEG2 layer 2, 256Kbps 0xD: MPEG2 layer 2, 320Kbps 0xE: MPEG2 layer 3, 96Kbps 0xF: AAC Bit[15:12]: Boot version 0=Golden Version 1=Update Version	R/W*
A2	Write: Bit[31:0]: 0x1234 = Start to update firmware bit image * Read: Bit[7:0]: Error count in received bit image Bit[23:12]: Current update address. 0xFFF=update done Bit[24]: bitimage_skip_erase Bit[25]: bitimage_receiving Bit[26]: biteimage_check_done Bit[27]: bitimage_check_ failed Bit[28]: bitimage_erase_running Bit[29]: bitimage_prog_running Bit[30]: bitimage_erase_done Bit[31]: bitimage_burn_done	R/W*
A9	Bit[0]: Reset DDR 1=keep DDR in reset. 0=Release DDR to run	R/W
A6	Bit[0]: Clock 200MHz locked Bit[1]: Encoder clock locked Bit[2]: DDR core calibration done Bit[3]: System reset from DDR core	R
F0	Bit[31:0]: Firmware Production Number	R
F1	Bit[31:0]: Firmware Git Revision	
FA	Bit[31:0]: Firmware Build Date	R
FB	Bit[31:0]: Firmware Build Time Stamp	R

Table-2: DDR Fifo Registers

The DDR fifo uses a portion of DDR to buffer update image. This allows for buffering of > 32Mbytes. The DDR fifo IP core is optional and not present in all designs. Please contact SOC if you feel this function is required for your application.

Note this core is not available for time-shared encoders at this time

Addr (HEX)	Information	Access
48	Bit[31:0]: Build Date	R
49	Bit[14]: Reset Bit[13]: Buffer Overflow Bit[10]: Byte Read Bit[9]: Output Buffer Empty Bit[8]: Output Buffer Ready Bit[3]: Timer Enabled* Bit[2]: Low Delay* Bit[1]: Clear Buffer Overflow Register* Bit[0]: API Reset*	R/W
4A	Bit[5:0]: Burst Size Bit[8]: Bypass DDR Fifo (DDR will not be used)	R/W
4B	Bit[25:0]: DDR Start Address	R
4C	Bit[25:0]: DDR End Address	R
4E	Bit[7:0]: DDR Buffer Percent	R
4E	Bit[7:0]: DDR Buffer Count (Number of Blocks in DDR)	R
4F	Bit[15:0]: Input Count	R

