SOC MCM 1000 MPEG2 Encoder

API Specification

Revision 1.2
2016.08.23

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Introduction

The API interface has 256 register (16 bit for writing and 32 bits for reading). Each register has an address to allow user-access. The registers accept command code for controlling the operation of the features within the FPGA. The registers may be read to acquire status and debugging information.

Some registers are allocated for user configurations and the rest are reserved for system functions such as debugging. The following table(s) specifies the address, definition, and access right (read/write) for the user-accessible registers. Note: registers of any API_TYPE that are NOT in the table are not designed for user access. If such a register is written to, the decoder may stop running. To recover, the core must be re-downloaded into the FPGA.

Control the API inside the FPGA

If it is necessary to control the API via the modules inside the FPGA, the ports of the API are available. Details, including the clock frequency, are provided in the corresponding integration manual.

Control the API outside the FPGA

If it is necessary to control the Decoder from outside the FPGA, the address, date, and R/W pins can be routed to the FPGA I/O pins. The desired FPGA I/O pins for the API may be selected or the SOC default pins may be used. An UART interface is available, upon request. The interface provides access to the API via uart_tx and uart_rx pins.

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Table-1 MPEG2 Core API registers description

Addr (HEX)	Information	Access
1	Bit[7:0]: GOP Size	R/W
3	Bit[1:0]: GOP Type - "00" = I + (GOPsize-1)P Frames - "10" = (GOPsize)P Frames with Intra Macroblocks -	R/W
4	Bit[3:0]: GOP Type 2 – Intra Macorblock Speed	R/W
10	Bit[1:0]: Chroma Format - "01" = 4:2:0 - "10" = 4:2:2	R/W
20	Version information: Bit[11:4] : sae number Bit[15:12]: DDR buffer row number Bit[19:16]: Search width Bit[23:20]: Search height Bit[27:24]: VLC_NUM Bit[28]: USE_B_FRAME	R

21	Bit[31:16]: Revision Only when Revision >= 0x0300, the registers 0x61~0x65 are valid.	R
61	Bit[31:0]: H264 Build Date	R
62	Bit[31:0]: H264 Build Time Stamp	R
64	Bit[31:0]: Production Number	R
65	Bit[31:0]: Firmware Git Revision	R
The register 70 to 7F control the bit rate and video quality Concept: Qp is the MPGE2 encoding quantization scale, range 0 to 31. The higher Qp value gets the worse encoding quality. Every macro block (16x16 pixel picture block in a frame) may have its own Qp to balance the bits and quality.		
70	Bit rate control bits: Bit[4:0] : reserved, don't change * Bit[10:3]: reserved, don't change Bit[11]: Control I frame, default '0', W1RB* When bit[11] is '0', the I frame is not controlled by bit rate control logic. Bit[12]: Control I slice, default '0', W1RB* When bit[12] is '0', the I slice is not controlled by bit rate control logic.	R/W
	Bit[13]: Initial adjust on, default '1', W1RB* If bit[13] is '1', the base Qp for frame is changed based on previous frames. Bit[14]: Use grad Qp adjustment, default '1', W1RB* Bit[15]: Reserved, W1RB* , don't write '1' to this bit.	
79	Bit[4:0]: Max Qp. The max qp control the worst block quality. The Max qp is bigger, the worst quality is worse but with lower bit number to encoding.	R/W
7F	Bit[15]: use user base Qp. Write x"8000" to reg 7F clear this bit. If bit[15] is '1', the bit[4:0] is used to control a frame as a base Qp. If bit[15] is '0', the encoder adjust the frame base Qp by bit-rate settings. Bit[4:0]: user base Qp. Writing this field (not zero and bit[15] is not '1') will set bit [15] to '1'.	R/W

Note:

(1) All the default values depend on the build version. So you may have different values for defaults.

(2) W1RB*: Write 1 Reverse Bit. The bit is reversed by writing logic '1'.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision	Author
24/11/2014	SOC initial Release	1.0	N/A
20/06/2016	Update to new firmware Added firmware revision registers: 0x20,0x21,0x61,0x62,0x64,0x65	1.1	Blake
23/-6/2016	Add register for bit-rate control: 0x70,0x79,0x7F	1.2	Blake