Video Input Core

API Specification

Revision 1.6
2017.9.26

Revision History

The following table shows the revision history for this document.

Date	Comment	Revision	Author
	Old versions	1.4	
09/14/2017	Added Revision History Added default values	1.5	Blake
09/26/2017	Corrected Register 0x80. Added 8K support, 0x8A, bit[17]	1.6	Blake

Default values

For writable register, default value is the value after power on. There is no default value for the states and information registers.

All default values depend on the build version and may be modified without notification.

Video Input Core

Addr (HEX)	Information	Access
92	Bit[2:0]: Multi-Channel/Time Sharing API Core Selection - 0 – Selects all cores for writing - 1-7 = Core # - Note only 1 core can be read at a time. A value of 0 should not be used for reading registers. Default value: 0. Depends on system level build, defined in "API - Encoder System API vn_n.pdf" (vn_n is version number).	R/W
The following registers are unique to each time-shared core (when used)		
80	Bit[15:12]: Supported Bit Depth	R
81	Bit[31:0]: Input module Build Date	R
82	Bit[31:0]: SOC Debug Register	R
83	Bit[11:0]: Width Override Default: 0 (no override)	R/W
84	Bit[11:0]: Height Override Default: 0 (no override)	R/W
85	Bit[31:16]: Active Height Bit[15:0]: Active Width	R
86	Bit[31:24]: Start of Frame Count (After Video Mode Selection) Bit[23:16]: End of Frame Count (After Video Mode Selection) Bit[15:8]: Start of Frame Count(Written to DDR) Bit[7:0]: End of Frame Count (Written to DDR)	R
87	Bit[8]: Frame Rate / 1.001 Detected Bit[7:0]: Frame Rate (Hz)	R
88	Bit[23:16]: Auto Frame Decimation - For Resolution/Frame rate restricted versions Bit[15:8]: Frame Rate Decimation Keep*	R/W*

	Bit[7:0]: Frame Rate Decimation* See note Frame Rate Decimation and Keep Default value: 0x00010000.	
89	Bit[15]: DDR Frame Available - Indicates there is an empty frame in DDR to write the current input video frame	R
8A	Bit[17]: 8K Frame Size Supported Bit[15]: Line Duplication Supported Bit[14]: Swap Interlaced Fields* Bit[13]: 4k Frame Size Supported Bit[12]: Clear all DDR frame Data* Bit[11]: Disable Input* Bit[10]: Disable Chroma* Bit[9]: Force DDR Frame Available* Bit[8]: Enable Watermark* Bit[6]: Enable Line Duplication* Bit[5]: Enable Horzontal Pixel Duplication* Bit[4]: Force Mode Dual Pixel Mode* Bit[3]: Force Mode Start/End of Line/Frame Format* Bit[2]: Force Mode HSync, VSync Format* Bit[1]: Force Mode TRS-EAV/SAV* Bit[0]: Force Mode BT-656* Default value: 0 for all applicable bits.	R/W*
8B	Bit[24:0]: Frame Length in (27Mhz Clock Cycles)	R
8C	Bit[15]: Interlaced Detected Bit[14]: Current Field Bit[13]: DE/Valid Detected Bit[12]: Dual Pixel Detected Bit[11]: TRS-EAV/SAV Detected Bit[10]: Start/End of Frame/Line Detected Bit[9]: Sync Mode Detected Bit[8]: BT656 Detected Bit[6:0]: DDR burst Size* Default: 0x20 (burst size=32)	R/W*
8D	Bit[31:24]: DDR Write Error Count Bit[23:16]: Frame Drop Count Bit[15:8]: Frame Bad/Damaged Count Bit[7:0]: Frame Ok Count	R
8E	Bit[13:12]: Crop Select - 00=Left - 01=Right	R/W

	- 10=Top - 11=Bottom Bit[11:0]: Crop Value Default: 0x0000. (No crop)	
8F	Bit[15]: BT656 Color Bar Test Pattern Enable*. Default '0'. Bit[8]: Video Locked - Indicated the Video is stable (Previous 2 frames have the same resolution+frame rate)	R/W*

Frame Rate Decimation and Keep

- Bit[7:0]: **D**ecimation specifies the frame grouping
- Bit[15:8]: **K**eep specifies how many frames to keep in the grouping
- Example: D=6, K=4 with an input frame rate of 60fps. Result in the following sequence where K is kept and D is dropped
    - KKKKDD, KKKKDD….
    - Resulting frame rate is 40fps.

