Datasheet – MPEG Video/Audio Codec Modules –NET Version

System-On-Chip (SOC) Technologies

Table of Contents

1. Overview of –NET Version Codec Modules

The –NET version of the SOC codec modules is a variation of the Standard codec modules, with the input of the decoder module and the output of the encoder module connected directly to an Ethernet PHY, while the standard encoder module has parallel pins for the TS (Transport Stream) output and the decoder module has parallel pins for inputting the TS. The hardware and electrical properties are all identical, except the pin assignments. Refer to the **Datasheet – MPEG Video/Audio Codec Modules – Standard Version** for details of SOC Codec Modules.

This Datasheet provides only the pin assignments for the –NET version modules for HD resolutions.

2. Pin Assignment for the –NET Version H.264/MPEG-2 HD Encoder Modules

The SOC SoM-X-A200T SoM is used for the –NET version of the H.264 and MPEG-2 HD encoder modules. The pin assignment and the signal voltages are provided in Table-1. The Artix-7 datasheet provides further information regarding the properties of these pins, and can be used as a reference. The product code of the Ethernet PHY used is 88E1111_BAB1C000

Table 1: H.264/ MPEG-2 HD Encoder Module (-NET version, based on SoM-A200T) Pin Assignment and Pin Voltages

Description	MCM-1000A Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
External Reset	121	Input	W21	3.3v	LVCMOS33
Video Clock	105	Input	Y11	3.3v	LVCMOS33
Video Horizontal Sync	146	Input	W16	3.3v	LVCMOS33
Video Vertical Sync	148	Input	V15	3.3v	LVCMOS33
Video Display Enable	150	Input	U15	3.3v	LVCMOS33
Video Data Luma[0]	50	Input	W14	3.3v	LVCMOS33
Video Data Luma[1]	52	Input	Y14	3.3v	LVCMOS33
Video Data Luma[2]	58	Input	V10	3.3v	LVCMOS33
Video Data Luma[3]	59	Input	Y13	3.3v	LVCMOS33
Video Data Luma[4]	60	Input	W10	3.3v	LVCMOS33
Video Data Luma[5]	61	Input	AA14	3.3v	LVCMOS33
Video Data Luma[6]	80	Input	AB13	3.3v	LVCMOS33
Video Data Luma[7]	82	Input	AA13	3.3v	LVCMOS33
Video Data Luma[8]	84	Input	AB17	3.3v	LVCMOS33
Video Data Luma[9]	86	Input	AB16	3.3v	LVCMOS33
Video Data Chroma[0]	92	Input	AA15	3.3v	LVCMOS33
Video Data Chroma[1]	94	Input	AB15	3.3v	LVCMOS33
Video Data Chroma[2]	96	Input	AB12	3.3v	LVCMOS33
Video Data Chroma[3]	98	Input	AB11	3.3v	LVCMOS33
Video Data Chroma[4]	107	Input	Y12	3.3v	LVCMOS33
Video Data Chroma[5]	108	Input	W12	3.3v	LVCMOS33
Video Data Chroma[6]	110	Input	Y17	3.3v	LVCMOS33
Video Data Chroma[7]	140	Input	T14	3.3v	LVCMOS33
Video Data Chroma[8]	142	Input	T15	3.3v	LVCMOS33

Video Data Chroma[9]	144	Input	W15	3.3v	LVCMOS33
SPDIF Audio	109	Input	Y21	3.3v	LVCMOS33
PHY_RXCLK	93	Input	Y18	3.3v	LCVMOS33
PHY_RXER	117	Input	AA19	3.3v	LCVMOS33
PHY_RXCTL_RXDV	95	Input	Y19	3.3v	LCVMOS33
PHY_RXD[0]	119	Input	AB20	3.3v	LCVMOS33
PHY_RXD[1]	101	Input	V17	3.3v	LCVMOS33
PHY_RXD[2]	103	Input	W17	3.3v	LCVMOS33
PHY_RXD[3]	91	Input	AA18	3.3v	LCVMOS33
PHY_RXD[4]	89	Input	AB18	3.3v	LCVMOS33
PHY_RXD[5]	85	Input	U17	3.3v	LCVMOS33
PHY_RXD[6]	87	Input	U18	3.3v	LCVMOS33
PHY_RXD[7]	97	Input	P14	3.3v	LCVMOS33
PHY_TXCLK	38	Input	V18	3.3v	LCVMOS33
PHY_TXC_GTXCLK	112	Output	AA20	3.3v	LCVMOS33
PHY_TXER	99	Output	R14	3.3v	LCVMOS33
PHY_TXCTL_TXEN	40	Output	V19	3.3v	LCVMOS33
PHY_TXD[0]	81	Output	R18	3.3v	LCVMOS33
PHY_TXD[1]	83	Output	T18	3.3v	LCVMOS33
PHY_TXD[2]	100	Output	P15	3.3v	LCVMOS33
PHY_TXD[3]	102	Output	R16	3.3v	LCVMOS33
PHY_TXD[4]	77	Output	N13	3.3v	LCVMOS33
PHY_TXD[5]	79	Output	N14	3.3v	LCVMOS33
PHY_TXD[6]	104	Output	P16	3.3v	LCVMOS33
PHY_TXD[7]	106	Output	R17	3.3v	LCVMOS33
PHY_RESET	139	Output	P19	3.3v	LCVMOS33
PHY_INT	123	Output	W22	3.3v	LCVMOS33
PHY_CRS	125	Input	U21	3.3v	LCVMOS33
PHY_COL	127	Input	T21	3.3v	LCVMOS33
UART_TX	90	Output	AA16	3.3v	LVCMOS33
UART_RX	88	Input	Y16	3.3v	LVCMOS33

3. Pin Assignment for the –NET Version H.264/ MPEG-2 HD Decoder Modules

The SOC SoM-X-A200T SoM is used for the –NET version of the H.264 and MPEG-2 HD decoder modules. The pin assignment and the signal voltages are provided in Table-2. The Artix-7 datasheet provides further information regarding the properties of these pins, and can be used as a reference. The product code of the Ethernet PHY used is 88E1111_BAB1C000

Table-2: H.264/MPEG-2 HD Decoder Module (-NET version, based on SoM-X-A200T) Pin Assignment and Pin Voltages

Description	MCM-1000A Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
External Reset	121	Input	W21	3.3v	LVCMOS33
Decoder Clock	115	Input	U20	3.3v	LVCMOS33
Video Clock	105	Output	Y11	3.3v	LVCMOS33
Video Horizontal Sync	146	Output	W16	3.3v	LVCMOS33

Video Vertical Sync	148	Output	V15	3.3v	LVCMOS33
Video Display Enable	150	Output	U15	3.3v	LVCMOS33
Video Data Luma[0]	50	Output	W14	3.3v	LVCMOS33
Video Data Luma[1]	52	Output	Y14	3.3v	LVCMOS33
Video Data Luma[2]	58	Output	V10	3.3v	LVCMOS33
Video Data Luma[3]	59	Output	Y13	3.3v	LVCMOS33
Video Data Luma[4]	60	Output	W10	3.3v	LVCMOS33
Video Data Luma[5]	61	Output	AA14	3.3v	LVCMOS33
Video Data Luma[6]	80	Output	AB13	3.3v	LVCMOS33
Video Data Luma[7]	82	Output	AA13	3.3v	LVCMOS33
Video Data Luma[8]	84	Output	AB17	3.3v	LVCMOS33
Video Data Luma[9]	86	Output	AB16	3.3v	LVCMOS33
Video Data Chroma[0]	92	Output	AA15	3.3v	LVCMOS33
Video Data Chroma[1]	94	Output	AB15	3.3v	LVCMOS33
Video Data Chroma[2]	96	Output	AB12	3.3v	LVCMOS33
Video Data Chroma[3]	98	Output	AB11	3.3v	LVCMOS33
Video Data Chroma[4]	107	Output	Y12	3.3v	LVCMOS33
Video Data Chroma[5]	108	Output	W12	3.3v	LVCMOS33
Video Data Chroma[6]	110	Output	Y17	3.3v	LVCMOS33
Video Data Chroma[7]	140	Output	T14	3.3v	LVCMOS33
Video Data Chroma[8]	142	Output	T15	3.3v	LVCMOS33
Video Data Chroma[9]	144	Output	W15	3.3v	LVCMOS33
Video Frame Sync Relock	56	Input	AB21	3.3v	LVCMOS33
SPDIF Audio	109	Output	Y21	3.3v	LVCMOS33
PHY_RXCLK	93	Input	Y18	3.3v	LCVMOS33
PHY_RXER	117	Input	AA19	3.3v	LCVMOS33
PHY_RXCTL_RXDV	95	Input	Y19	3.3v	LCVMOS33
PHY_RXD[0]	119	Input	AB20	3.3v	LCVMOS33
PHY_RXD[1]	101	Input	V17	3.3v	LCVMOS33
PHY_RXD[2]	103	Input	W17	3.3v	LCVMOS33
PHY_RXD[3]	91	Input	AA18	3.3v	LCVMOS33
PHY_RXD[4]	89	Input	AB18	3.3v	LCVMOS33
PHY_RXD[5]	85	Input	U17	3.3v	LCVMOS33
PHY_RXD[6]	87	Input	U18	3.3v	LCVMOS33
PHY_RXD[7]	97	Input	P14	3.3v	LCVMOS33
PHY_TXCLK	38	Input	V18	3.3v	LCVMOS33
PHY_TXC_GTXCLK	112	Output	AA20	3.3v	LCVMOS33
PHY_TXER	99	Output	R14	3.3v	LCVMOS33
PHY_TXCTL_TXEN	40	Output	V19	3.3v	LCVMOS33
PHY_TXD[0]	81	Output	R18	3.3v	LCVMOS33
PHY_TXD[1]	83	Output	T18	3.3v	LCVMOS33
PHY_TXD[2]	100	Output	P15	3.3v	LCVMOS33
PHY_TXD[3]	102	Output	R16	3.3v	LCVMOS33
PHY_TXD[4]	77	Output	N13	3.3v	LCVMOS33
PHY_TXD[5]	79	Output	N14	3.3v	LCVMOS33
PHY_TXD[6]	104	Output	P16	3.3v	LCVMOS33
PHY_TXD[7]	106	Output	R17	3.3v	LCVMOS33
PHY_RESET	139	Output	P19	3.3v	LCVMOS33
PHY_INT	123	Output	W22	3.3v	LCVMOS33
PHY_CRS	125	Input	U21	3.3v	LCVMOS33
PHY_COL	127	Input	T21	3.3v	LCVMOS33
UART_TX	90	Output	AA16	3.3v	LVCMOS33
UART_RX	88	Input	Y16	3.3v	LVCMOS33