System-On-Chip Technologies

Specification Sheet

H.264 Video Decoder IP Core

Product Description

SOC provides the H.264 decoder in three formats: IP cores for FPGAs, ASIC chipsets, and standalone all-in-one modules.

IP cores are available for both Xilinx and Altera FPGAs. SOC configures the cores according to user specifications, including I/O formats.

The SOC codec chipsets (SOC-Mcodec™) are AISC chips based on the SOC IP cores. Standard H.264 decoder chipsets for different specifications are available.

The SOC codec modules are System-on-Module (SoM) cards, based on SOC codec IP cores, that can be connected to user devices/PCBs using a standard DDR3 memory connector.

Users have the options of using the codec IP cores, chipsets, or modules. If IP cores are preferred, users have the option of Xilinx or Altera FPGAs.

SOC also offers product development boards, which allow users to develop products using the SOC codec IP core, chipsets, and modules.

Key Features

- All-hardware design (without embedded processors)
- High Speed (Low latency)
- Small Silicon Footprint
- Low Power
- High Reliability (due to hardware architecture)
- High-Precision – 10bits available
- High-Video Quality
- Decode streams with any bit rate
- User controllable API
- Option of IP Core or Module
- Video Transmission Cores available
- Development Board available

Specifications

- Standard: H.264/AVC (ISO/IEC14496-10)
- Profiles: High, up to level 4.1
  Support lower profiles
- Video resolutions: Up to 1080i/p
- Frame rate: Up to 60fps
- Chroma formats: 4:2:2 or 4:2:0
- Precision: 8 bits or 10 bits
- Input format: H.264 Elementary, or
  Transport Stream
- Video output format: RGB or YUV
- Audio support: AAC or MPEG-2 Layer-II
- Latency: 0.25ms
- Power consumption: 800mw (IP core)
- FPGAs: Xilinx or Altera

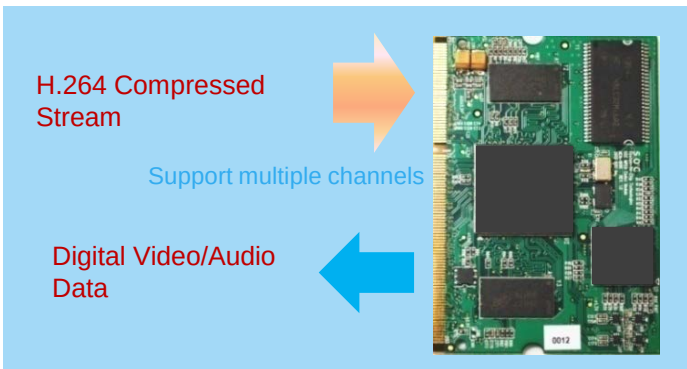
FPGA Resources

	Xilinx FPGAs	Altera FPGAs
Logic Resources:	45,000 LUTs	30,000 ALMs
Block RAMs:	3,000kb	2,500kbits
DSPs:	25 DSPs	25 DSPs

H.264 Video/Audio Decoder Chipset

SOC-Mcodec™

H.264 Video/Audio Decoder Module



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