

## MPEG-2 Video Encoder IP Core

### Product Description

SOC provides the MPEG-2 encoder in three formats: IP core for FPGAs, ASIC Chipset, and a standalone all-in-one modules.

IP cores are available for both Xilinx and Altera FPGAs. SOC configures the cores according to user specifications, including I/O formats.

The SOC codec chipsets are ASIC chips based on the SOC IP cores. Standard MPEG-2 encoder chipsets for different specifications are available.

The SOC codec modules are System-on-Module (SoM) cards, based on the SOC codec IP cores, that can be connected to user devices/PCBs using a standard DDR3 memory connector.

Users have the options of using the one of these product formats, based on the applications.

SOC also offers product development boards, which allow users to develop products using the SOC MPEG-2 video/audio encoder IP cores, chipsets, or modules.

### Key Features

- All-hardware design (no embedded software)
- High Speed (Low latency)
- Small Silicon Footprint
- Low Power
- High Reliability (due to hardware architecture)
- High-Video Quality
- Low Output Bandwidth
- High-Output Bandwidth Version Available
- User controllable API
- Option of IP Core, Chipset or Module
- Video Transmission (Network) Cores available
- Development Board available

### IP Core Specifications

- Standard: MPEG-2/H.262 (ISO/IEC 13818)
- Profiles: High, Main, Baseline
- Output bit rates: 1-100Mbps & above
- Video resolutions: Up to 1080i/p
- Frame rate: Up to 60fps
- Chroma formats: 4:2:2 or 4:2:0
- Output format: MPEG-2 Elementary, or Transport Stream
- Video input format: RGB or YUV
- Audio support: MPEG-2 Layer-II or AAC
- Latency: 0.25ms
- Power consumption: 0.8w (IP core)
- FPGAs: Xilinx or Altera

### FPGA Resources

	Xilinx FPGAs	Altera FPGAs
Logic Resources:	90,000 LUTs	6,000 ALMs
Block RAMs:	7,000kb	5,000kbits
DSPs:	320 DSPs	310 DSPs

### MPEG-2 Video/Audio Encoder Chipset



### MPEG-2 Video/Audio Encoder Module

