SOC H.264 AVC 4k Video Decoder Datasheet

System-On-Chip (SOC) Technologies

1. Key Features

1. Profile: High profile
2. Resolution: 4k (3840x2160)
3. Frame Rate: up to 30fps
4. Chroma Format: 4:2:0 or 4:2:2
5. Precision: 8 or 10 bits
6. Input Stream: Transport or Elementary
7. Latency: 0.25ms

2. Product Overview

The SOC H.264 AVC 4k video decoder is a single chip solution that supports single or multi-stream H.264 4k (3840x2160) video decoding up to 30fps.

SOC provides the versions of the H.264 4k video encoder IP core for FPGAs of both Xilinx, and Altera. SOC also supplies an all-in-one 4k decoder module based on this H.264 4k video decoder IP core. Refer to the Product Brief and Datasheet for SOC MPEG codec modules for details.

The SOC H.264 AVC 4k video decoder is implemented based on SOC's proprietary single-clock driven all-hardware technology (without microprocessors or embedded software), which has significant advantages of high-speed (low latency), small footprint (low power), high video quality, and high resolution.

The SOC H.264 AVC 4k video decoder is at high-profile and backward compatible with main and simple profiles according to the MPEG standard. It decodes both 4:2:0 and 4:2:2 streams with automatic selection. The decoder is suited for both consumer products and high-end applications such as broadcast, digital cinema, and medical devices.

The SOC decoder series can be integrated with an audio decoder to provide an all-in-one decoding solution. SOC also integrates network modules, TCP/UDP-IP, Ethernet MACs, as well as the MPEG transport de-multiplexer into the design to produce full system-on-chip systems. Customized versions of these products are available on request.

3. The SOC H.264 AVC 4k Video Decoder Architecture

The SOC H.264 4k video decoder has the same architecture of HD/SD decoder. Fig. 1 is the block diagram of the SOC H.264 AVC video decoder. It is a self-contained FPGA IP core that can be either placed into a single FPGA or integrated with other logic blocks in the same FPGA for system-on-chip solutions.

All of the blocks in the design, shown in Fig. 1, are implemented in hardware without embedded processors or embedded software, which offers high speed, low logic resource consumption, and low power. Input to the decoder is standard H.264 elementary stream without bit rate limitation. The output of the decoder is the video stream for standard display devices with frames properly ordered. SOC also provides an MPEG transport decoder to allow the input to the decoder to be in the form of MPEG transport streams.

The decoder also automatically detects missing data, if any, and compensates for the missing blocks using the corresponding blocks in the neighboring frames to increase the overall video quality.

The SOC H.264 video decoder requires two external clock sources with one at 100MHz and the second at 27MHz. The decoder also requires an external DDR3 memory of minimum of 1GB for 4k resolution.

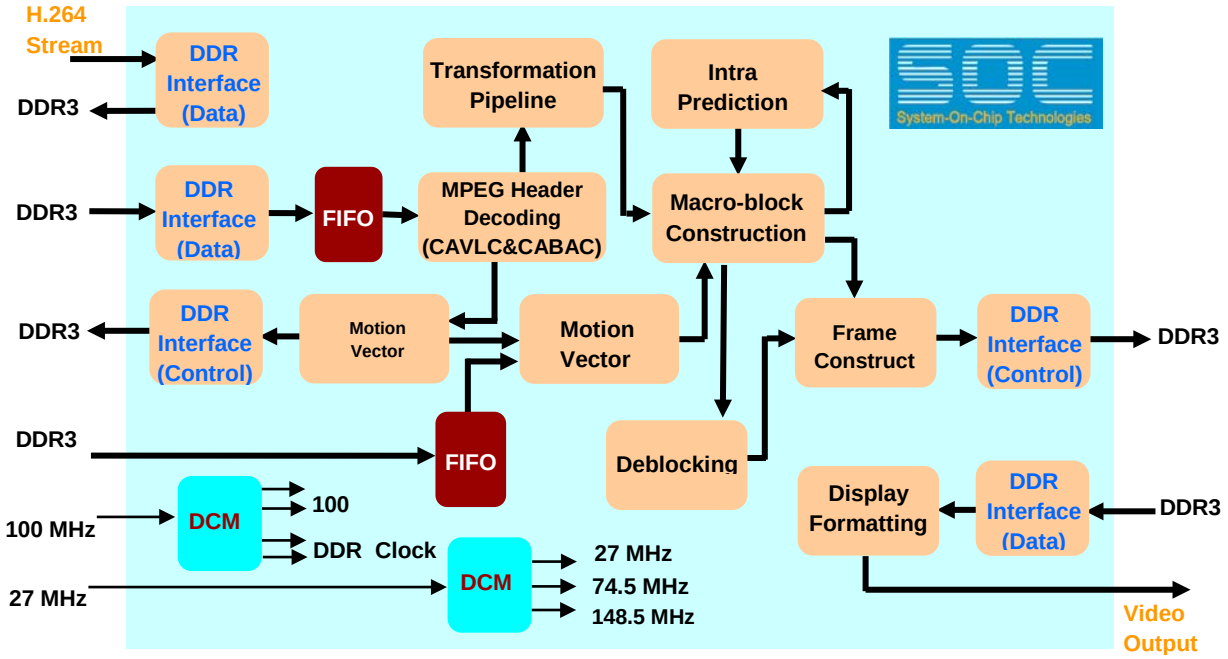

Fig. 1 The SOC H.264 decoder architecture

4. Technical Specifications

Conformance Standard:

H.264/AVC (ISO/IEC14496-10)

Profile:

- Simple Profile
- Main Profile, and
- High Profile.

Chroma Format:

- 4:2:0
- 4:2:2
- 4:4:4 (on request)

Precision:

- 8 bits
- 10 bits.

Inter Frames:

- I frame
- P frame
- B frame.

Frame Rates:

- 10fps, 24fps, 25fps, 29.97fps, 30fps
- 50fps, 59.95fps, 60fps

Input Data Rate:

There is no limitation on the data rate of the input streams, as long as it is H.264 compliant.

Latency:

The SOC H.264 video decoder has very low latency due to its hardware implementation. The decoding engine latency is less 0.25ms from data in to data out. The decoder can buffer 1 complete frame before display, if needed, to compensate any jitters of the input stream, which is controllable through the API.

Power:

The power consumption is less than 1.0w for the core only.

5. Targeted FPGAs

The SOC H.264 4k video decoder IP core is customized for both Xilinx and Altera FPGAs, including:

- Kitex-7
- Zynq-7
- KintexUltrascale
- Arria-V
- Arria-10
- Stratix-IV
- Stratix-V

6. The H.264 4k Video Decoder Integration Sheet

When the 4k decoder is delivered in IP core format, it is a ready-to-use bit-stream core for FPGAs. SOC supports Xilinx FPGAs. Fig. 2 shows the inputs and outputs of the decoder core.

The H.264 4k video decoder IP core integration details are provided in a separate document under the title of "H.264 4k Video Decoder IP Core Integration Sheet".

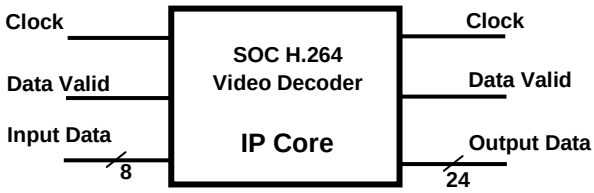

Fig. 2 The inputs and outputs of the H.264 IP Core

7. The H.264 4k Decoder Module

SOC supplies the H.264 4k decoder on a 2.7"x2.0" module (card), as shown in Fig. 3. The module provide complete function of 4k video/audio decoding. The module connects to the host product/PCB via a device-to-PCB connector, as shown in Fig. 4.

Refer to the Product Brief and Datasheet of SOC MPEG Codec Modules for technical details.

Fig. 3 SOC MPEG Codec Module

Fig. 4. Device-to-PCB connectors

8. Technical Support

SOC provides technical support for all its products, which include documentation, web site based, and telephone based support. Additional support services, such as on-site training services, can be subscribed from SOC as a service contract.

9. IP core upgrading

An upgrade is usually a part of the technical support contract signed individually. Upgrade programs can be subscribed after the technical support period. On-line automatic upgrading can also be arranged if desirable.

10. Ordering Information

The SOC H.264 4k video/audio decoder IP cores are available for licensing or a combination of one-time fee plus reduced royalty payments.

Please contact SOC sales by telephone +1 519 880-8609 or e-mail: sales@soctechnologies.com