System-On-Chip Technologies

Specification Sheet

H.265 4k Video Encoder IP Core

Product Description

SOC provides the H.265 4k encoder in three formats: IP cores for FPGAs, ASIC Chipsets, and all-in-one hardware modules.

IP cores are available for both Xilinx and Altera FPGAs. SOC also configures the cores according to user specifications, including I/O formats.

The SOC codec chipsets (SOC-Mcodec™) are AISC chips based on the SOC IP cores. Standard H.265 encoder chipsets for different specifications are available.

The SOC codec modules are System-on-Module (SoM) cards, based on SOC codec IP cores, that can be connected to user devices/PCBs using a standard DDR3 SODIMM connector.

Users have the options of using the codec IP cores, chipsets, or modules. If IP cores are preferred, users have the option of Xilinx or Altera FPGAs.

SOC also offers product development boards, which allow users to develop products using the SOC codec IP core, chipsets, and modules.

Key Features

- All-hardware Design (without embedded processors)
- High Speed (Low latency)
- Small Silicon Footprint
- Low Power
- High Reliability (due to hardware architecture)
- High-Precision – 10bits available
- High-Video Quality
- Low Output Bandwidth
- High-Output Bandwidth Version Available
- User Controllable API
- Option of IP Core or Module
- Video Transmission Cores available
- Development Board available

Specifications

- Standard: H.265/HEVC (ISO/IEC 23008-2:2015)
- Video Encoder Profiles: Main 8, 10
- Output Bit Rates: 2-100Mbps & above
- Video Resolutions: 4K@30, 4k@60
- Chroma Formats: 4:2:2 or 4:2:0
- Precision: 8/10bits
- Output Format: H.265 Elementary, or Transport Stream
- Video Input Format: RGB or YUV
- Audio Support: AAC or MPEG-2 Layer-II
- Latency: 0.5ms
- Power Consumption: 4-12w (Core only)
- Target FPGAs: Xilinx or Intel

FPGA Resources for 4k@30

	Xilinx FPGAs	Intel FPGAs
Logic Resources:	180k LUTs	120k ALMs
Block RAMs:	16Mbits	16Mbits
DSPs:	375 DSPs	375 DSPs

FPGA Resources For 4k@60

The logic resources for 4k@60 equal to twice of the resources of the 4k@30, as two 4k@30 engines are used to achieve the 4k@60 resolution.

H.265 Video/Audio Encoder Chipset

SOC-MCodec™

H.265 Video/Audio Encoder Module

Digital Video/Audio Data

Support multiple channels

H.265 Compressed Video/Audio Stream

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