System-On-Chip Technologies

Specification Sheet

H.265 HD Video Encoder IP Core

Product Description

SOC provides High-performance H.265/HEVC encoder IP cores for both Xilinx and Intel (Altera) FPGAs. SOC also configures the cores according to user specifications, including I/O formats.

SOC also supplies all-in-one hardware modules and ASIC Chipsets, based on the IP cores.

The SOC codec modules are System-on-Module (SoM) cards, based on SOC codec IP cores, that can be connected to user devices/PCBs using a standard DDR3 memory connector.

Users have the options of using the codec IP cores, chipsets, or modules.

Plug-and-play evaluation kits are available for the IP cores, modules, and chipsets.

SOC also offers product development boards, which allow users to develop products using the SOC codec IP core, chipsets, and modules.

Key Features

- All-hardware Design (without embedded processors)
- High Speed (Low latency)
- Small Silicon Footprint
- Low Power
- High Reliability (due to hardware architecture)
- High-Precision – 10bits available
- High-Video Quality
- Low Output Bandwidth
- High-Output Bandwidth Version Available
- User Controllable API
- Option of IP Core or Module
- Video Transmission Cores available
- Development Board available

Specifications

- Standard: H.265/HEVC (ISO/IEC 23008-2:2015)
- Video Encoder Profiles: Main 8, 10
- Output Bit Rates: 1-100Mbps & above
- Video Resolutions: HD 1080p up to 60fps
- Chroma Formats: 4:2:2 or 4:2:0
- Precision: 8 /10 bits
- Output Format: H.265 Elementary, or Transport Stream
- Video Input Format: RGB or YUV
- Audio Support: AAC or MPEG-2 Layer-II
- Latency: 0.25ms
- Power Consumption: 2-4w (Core only)
- Target FPGAs: Xilinx or Intel

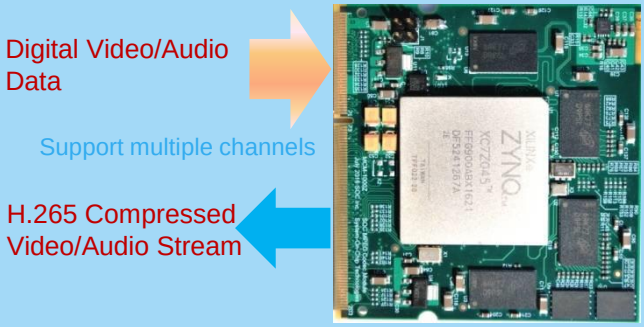
FPGA Resources

	Xilinx FPGAs	Intel FPGAs
Logic Resources:	180k LUTs	120k ALMs
Block RAMs:	10Mbits	10Mbits
DSPs:	450 DSPs	450 DSPs

H.265 Video/Audio Encoder Chipset

SOC-MCodec™

H.265 Video/Audio Encoder Module



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