System-On-Chip Technologies

Specification Sheet

MPEG-2 Video Decoder IP Core

Product Description

SOC provides the MPEG-2 decoder in Three formats: IP cores for FPGAs, ASIC Chipsets, and a standalone all-in-one modules.

IP cores are available for both Xilinx and INTEL (Altera) FPGAs. SOC configures the cores according to user specifications, including I/O formats.

The SOC codec chipsets (SOC-Mcodec) are ASICs based on the SOC codec IP cores.

The SOC MPEG video/audio codec modules are System-on-Module (SoM) cards that can be connected to a user devices/PCBs using a standard DDR3 memory connector.

Users have the options of using the IP cores, chipsets, and modules. If IP cores are preferred, users have the option of Xilinx or Altera FPGAs.

SOC also offers product development boards, which allow users to develop products using the SOC MPEG-2 video/audio decoder IP cores or modules.

Key Features

- All-hardware Design (Without embedded processors)
- High Speed (Low latency)
- Small Silicon Footprint
- Low Power
- High Reliability (due to hardware architecture)
- High-Video Quality
- Automatic adapting profiles
- Up to 60fps
- User controllable API
- Option of IP Core or Module
- Video Transmission (Network) Cores available
- Development Board available

Specifications

- Standard: MPEG-2/H.262 (ISO/IEC 13818)
- Profiles: High, Main, Baseline
- Input bit rates: Up to 100Mbps & above
- Video resolutions: Up to 1080i/p
- Frame rate: Up to 60fps
- Chroma formats: 4:2:2 or 4:2:0
- Input format: MPEG-2 Elementary, or Transport Stream
- Video output format: RGB or YUV
- Audio support: MPEG-2 Layer-II or AAC
- Latency: 0.25ms
- Power consumption: 0.7w (IP core)
- FPGAs: Xilinx or Altera.

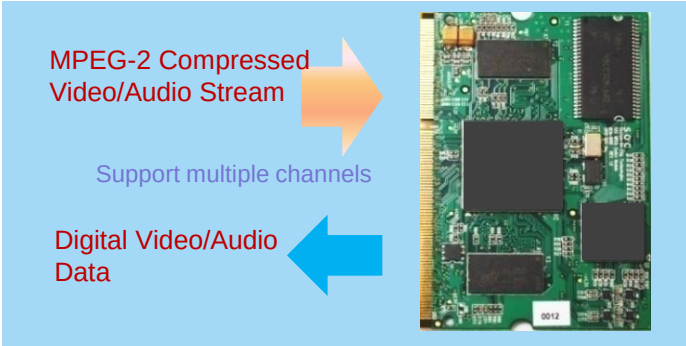
FPGA Resources

	Xilinx FPGAs	Altera FPGAs
Logic Resources:	12,000 LUTs	8,500 ALMs
Block RAMs:	756kb	650kbits
DSPs:	54 DSPs	54 DSPs

MPEG-2 Video/Audio Decoder Chipset

SOC-Mcodec™

MPEG-2 Video/Audio Decoder Module



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