Datasheet - MPEG Video/Audio Codec Chipset

SOC-MCodec™

System-On-Chip (SOC) Technologies

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1. Product Overview

1.1 Overview of SOC Codec Chipsets

The SOC MPEG Codec Chipsets are based on off-the-shelf FPGAs and SOC codec IP cores. The SOC IP cores are pre-stored into a Flash Memory for the target FPGA chip. The FPGA and the pre-configured Flash Memory form the chipset – the SOC MCodec family SOC-MCodec™. Customers can purchase both the FPGA and the pre-configured flash memory chip from SOC or purchase the pre-configured flash memory only. In the case of purchasing the pre-configured flash memory only from SOC, the customer may purchase the target FPGA chips from the FPGA vendors directly. It should also be noted that an IP core key, which is a pre-written (3mmX3mm) EEPROM, comes with the flash memory as well, for IP protection.

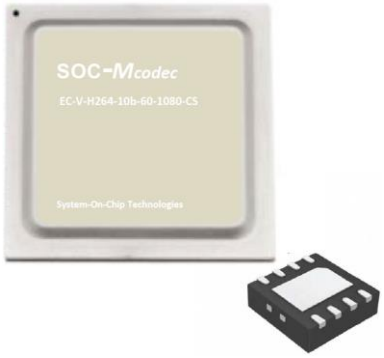

Fig. 1 The SOC Encoder chipset

Fig. 2 The SOC decoder chipset

The codec chipsets are available for the following categories:

1. H.265 HD and 4K Video/Audio Encoders;
2. H.265 HD and 4k Video/Audio Decoders (to come in 2019);
3. H.264 HD and 4K Video/Audio Encoders;
4. H.264 HD and 4K Video/Audio Decoders;
5. MPEG-2 HD Video/Audio Encoders;
6. MPEG-2 HD Video/Audio Decoders;
7. H.264-to-H.265 Transcoders;
8. MPEG2-to-H.264 Video/Audio Transcoders;
9. H.264-to-MPEG2 Video/Audio Transcoders;
10. Multiple-channel Encoder and/or Encoders/Decoders (Special order);
11. Multiple-standard Encoder and/or encoders/Decoders (Special order).

In each of the above categories, a series of standard chips are offered for different applications, from lower-end to high-end. Specifications for standard chips, such as resolution and frame rate, are provided in Appendix-A.

Since the chipsets use the SOC codec IP cores, the technical and performance details for the encoder, decoder, and transcoder chipsets are provided in the Datasheets of the IP cores that are used to configure the chips, which are:

- Datasheet – H.265 HD Encoder IP Cores
- Datasheet – H.265 4k Encoder IP Cores

- Datasheet – H.264 HD Encoder IP Cores
- Datasheet – H.264 4kEncoder IP Cores

- Datasheet – H.264 HD Decoder IP Cores
- Datasheet – H.264 4k Decoder IP Cores

- Datasheet – MPEG-2 Encoder IP Cores

- Datasheet – MPEG-2 Decoder IP Cores

- Datasheet – H.265-to-H.264 Transcoder IP Cores

- Datasheet – MPEG-2-to-H.264 Transcoder IP Cores

- Datasheet – H.264-to-MPEG-2 Transcoder IP Cores

User interface for controlling the operations of the chips are provided by the API interface manual:

- API Manual - H265 Encoder IP Cores
- API Manual - H264 Encoder IP Cores
- API Manual - H264 Decoder IP Cores
- API Manual – MPEG-2 Encoder Cores
- API Manual – MPEG-2 Decoder Cores

Information for integrating the chips on to user PCBs are provided in this datasheet. SOC also provides PCB design references through its licensing programs. Contact SOC sales for details: sales@soctechnologies.com

For each chipset, one of SOC SOM module designs is provided to the customers as a PBC design reference (MOQ is required). The SOC SOM modules have all of required components for SOM application, including DDR memory, flash memory, clocks, etc. SOC configures the SOMs into Codec Modules using the same IP cores for the Chipsets.

1.2 Product Code for SOC Codec Chipsets

The SOC codec chipsets are pre-configured flash memory chip plus the target FPGA chip, using one of the SOC codec IP cores (encoder, decoders, and transcoders, etc). SOC offers a series of MPEG codec chipsets as standard products. Fig. 3 shows the product code format for the SOC MPEG codec chipsets. The same product code format is used for the SOC codec IP cores, codec modules, and codec chipsets.

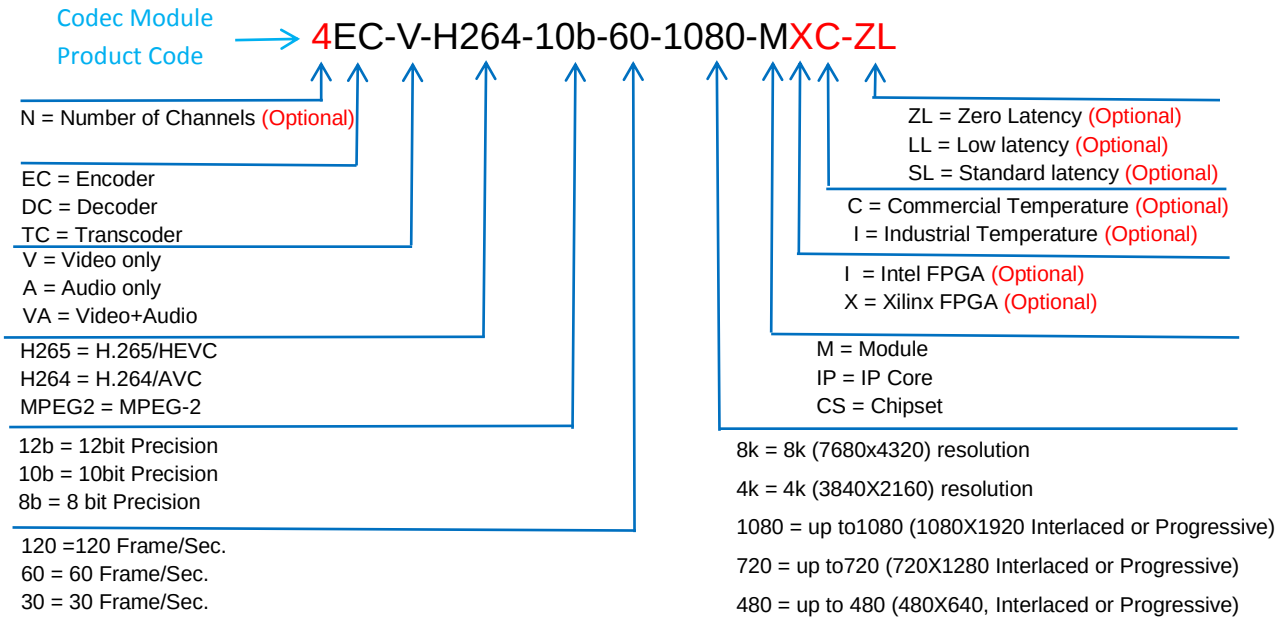

Fig. 3. The SOC Codec IP core, Codec Module, and Chipset product code format

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2. The H.264 (or MPEG-2) HD Encoder Chipset

2.1 Pin Assignments and Pin Voltages

The HD encoder chipset for H.264 or MPEG-2 has the same pin assignments and electrical properties. The FPGA used is the Xilinx Artix-7 XC7A200T-SBG484. The flash memory is the Micron N25Q256A13EF840F (or compatible).

In order to enable quick PCB design for the customers, SOC provides a full working design – the SOC SOM module based on the XC7A200T-SBG484 (SOC Product Code for the module is: SoM-X-A200T). The SoM-X-A200T schematics under licensing? will come with the first shipment of chipset. Information regarding the SoM-X-A200T and the SOC MPEG Codec modules based on the SoM-X-A200T can be found in:
Datasheet – MPEG Video/Audio Codec Modules– Standard Version (V.4.0, 2019)

Table-1 lists the pin assignments and pin voltages for H.264 (or MPEG-2) HD video encoder chipset based on the XC7A200T-SBG484. The pin number for the SoM-X-A200T connected to the FPAG pins are also provided in Table-1. Refer to Appendix-B for the edge pin schematics of the SoM-X-A200T. Further details can be found in the SoM-X-A200T full schematics, which comes with the first chipset shipment.

Table 1: H.264 (or MPEG-2) HD Encoder Chipset (based on Artix-7 XC7A200T-SBG484 FPGA) **Pin Assignment and Pin Voltages**

Description	SoM-X-A200T Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
Video Clock	105	Input	AB15	3.3V	LVCMOS33
Video Horizontal Sync	133	Input	M18	1.5V	LVCMOS15
Video Vertical Sync	113	Input	AB17	3.3V	LVCMOS33
Video Display Enable	67	Input	J15	1.5V	LVCMOS15
Video Data Luma[0]	135	Input	N20	1.5V	LVCMOS15
Video Data Luma[1]	137	Input	N19	1.5V	LVCMOS15
Video Data Luma[2]	116	Input	G15	1.5V	LVCMOS15
Video Data Luma[3]	118	Input	H15	1.5V	LVCMOS15
Video Data Luma[4]	124	Input	G16	1.5V	LVCMOS15
Video Data Luma[5]	126	Input	J16	1.5V	LVCMOS15
Video Data Luma[6]	128	Input	J17	1.5V	LVCMOS15
Video Data Luma[7]	130	Input	H17	1.5V	LVCMOS15
Video Data Luma[8]	132	Input	G18	1.5V	LVCMOS15
Video Data Luma[9]	134	Input	N18	1.5V	LVCMOS15
Video Data Chroma[0]	143	Input	L18	1.5V	LVCMOS15
Video Data Chroma[1]	145	Input	M20	1.5V	LVCMOS15
Video Data Chroma[2]	147	Input	L19	1.5V	LVCMOS15
Video Data Chroma[3]	149	Input	L20	1.5V	LVCMOS15
Video Data Chroma[4]	151	Input	K18	1.5V	LVCMOS15
Video Data Chroma[5]	153	Input	K19	1.5V	LVCMOS15
Video Data Chroma[6]	155	Input	J20	1.5V	LVCMOS15
Video Data Chroma[7]	157	Input	J21	1.5V	LVCMOS15
Video Data Chroma[8]	159	Input	J19	1.5V	LVCMOS15
Video Data Chroma[9]	161	Input	H19	1.5V	LVCMOS15

SPDIF Audio	27	Input	G13	1.5V	LVCMOS15
Transport Stream Buffer Ready	29	Input	H13	1.5V	LVCMOS15
Transport Stream Clock	31	Output	H14	1.5V	LVCMOS15
Transport Stream Data Valid	33	Output	J14	1.5V	LVCMOS15
Transport Stream Data[0]	152	Output	B20	3.3V	LVCMOS33
Transport Stream Data[1]	154	Output	C19	3.3V	LVCMOS33
Transport Stream Data[2]	158	Output	A19	3.3V	LVCMOS33
Transport Stream Data[3]	160	Output	A18	3.3V	LVCMOS33
Transport Stream Data[4]	162	Output	T18	3.3V	LVCMOS33
Transport Stream Data[5]	164	Output	T20	3.3V	LVCMOS33
Transport Stream Data[6]	166	Output	T19	3.3V	LVCMOS33
Transport Stream Data[7]	156	Output	A20	3.3V	LVCMOS33
Uart_tx	90	Output	U18	3.3V	LVCMOS33
Uart_rx	88	Input	Y12	3.3V	LVCMOS33

2.2 Signal Formats

2.2.1 Video Clock Signal (Input)

The **Video Clock** signal has two functions: (1) It is the clock for the input video data, and (2) it is the clock that drives the encoder engine.

The **Video Clock** signal usually comes from the video input interface chip, such as HDMI or SDI. It is the clock for the input video data. It is also used for driving the encoder engine. A local clock source (e.g. oscillator) is required to drive the video input interface chip. The frequency varies according to the resolution of the video input. The following are the clock frequencies for standard video resolutions.

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60

2.2.2 Video Data Signals (Input)

The input to the encoder FPGA chip (H.264 or MPEG-2) is raw video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma. And, 10 input lines: **Video Data Chroma[0]** to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]** , **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros. All of the Video Data signals are single-ended.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization. A **Video Clock** coming from the video interface chip (refer to Section **2.2.1** for the clock frequencies) is required to provide the timing for the parallel input of luma, chroma, as well as for the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Display Enable signal** at high, when active pixels are

being sent out. The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section **2.2.1.**

2.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

2.2.4 TS stream Signals (Output)

The output of the encoder chip is MPEG Transport Stream (TS), which is sent out from the chip by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7];** along with the Transport Stream output data clock **Transport Stream Clock**. The frequency of the Transport Stream Data clock is 27MHz.

Transport Stream Buffer Ready and **Transport Stream Data Valid** are the signals to inform the user side to take over the signals.

2.2.5 Encoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the encoder. **Uart_rx** receives the command from an external control device. **Uart_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Encoder API User Manual for more details.

2.3 Power Supplies to the FPGA Chip

Refer to the FPGA chip datasheet for the power supplies required. A power rail system reference design can be found in the SOC codec module datasheet, in Section **4.3 Power Rails of SoM-X-A200T** of Datasheet – MPEG Video/Audio Codec Modules– Standard Version (V.4.0, 2019)

The total power, at operation, required by a given encoder module ranges from 2 to 5 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails (including DDR memory), each individual power rail delivers only a portion of the total power. However, the power is not evenly distributed among the rails. Table-2 provides a power estimation for each rail for the carrier board PCB design purpose.

Table-2: Power supply estimation for the encoder chip for PCB design

Power Rail	Current (A)	Power (W)
3.3V	0.23	0.76
2.5V	0.62	1.55
1.5V	0.78	1.16
1.3V	0.23	0.30
1.2V	0.47	0.57
1.0V	2.12	2.12

Since the encoder FPGA chip normally shares the power supplies with the PCB board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 10 of this document. The reference designs provide not only the power system design and clock distributions, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: sales@soctechnologies.com for design licensing details.

2.4 FPGA Booting Sequence

The SOC codec IP core in the FPGA does not require special booth sequence, as long as the FPGA is booted. Refer to the FPGA data sheet for booting sequence design.

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3. The H.264 (and MPEG-2) HD Decoder Chipset

3.1 Pin Assignments and Pin Voltages

The decoder for H.264 or MPEG-2 has the same pin assignment. The chipset for HD resolution decoder uses the Artix-7 XC7A200T-SBG484 FPGA as well (the same as the one used for the HD Encoder). The flash memory is also the same as the one used in the encoder chipset, which is N25Q256A13EF840F (or compatible).

This section details the pin assignments and pin voltages for the HD decoder (H.264 or MPEG-2) chipset, which are listed in Table-3. Again, the SOC SOM: SoM-X-A200T is used as a reference PCB design. The SoM-X-A200T schematics for the edge pins is provided in Appendix-B. Full schematics of the SoM-X-A200T comes with the first decoder chipset shipment. Information regarding the SoM-X-A200T and the SOC MPEG Codec Modules based on the SoM-X-A200T can be found in:
Datasheet – MPEG Video/Audio Codec Modules – Standard Version (V.4.0, 2019)

It should be noted that the HD encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder become the video output pins on the decoder.

Table-3: H.264 HD Decoder chipset (based on Artix-7 XC7A200T-SBG484 FPGA**) Pin Assignment**

Description	SoM-X-A200T Edge Connector	Direction	FPGA Pin #	Voltage	IO Standard
Decoder Clock	80	Input	R17	3.3V	LVCMOS33
Use Decoder Clock	63	Input	L14	1.5V	LVCMOS15
Video Clock	105	Output	AB15	3.3V	LVCMOS33
Video Horizontal Sync	133	Output	M18	1.5V	LVCMOS15
Video Vertical Sync	113	Output	AB17	3.3V	LVCMOS33
Video Display Enable	67	Output	J15	1.5V	LVCMOS15
Video Data Luma[0]	135	Output	N20	1.5V	LVCMOS15
Video Data Luma[1]	137	Output	N19	1.5V	LVCMOS15
Video Data Luma[2]	116	Output	G15	1.5V	LVCMOS15
Video Data Luma[3]	118	Output	H15	1.5V	LVCMOS15
Video Data Luma[4]	124	Output	G16	1.5V	LVCMOS15
Video Data Luma[5]	126	Output	J16	1.5V	LVCMOS15
Video Data Luma[6]	128	Output	J17	1.5V	LVCMOS15
Video Data Luma[7]	130	Output	H17	1.5V	LVCMOS15
Video Data Luma[8]	132	Output	G18	1.5V	LVCMOS15
Video Data Luma[9]	134	Output	N18	1.5V	LVCMOS15
Video Data Chroma[0]	143	Output	L18	1.5V	LVCMOS15
Video Data Chroma[1]	145	Output	M20	1.5V	LVCMOS15
Video Data Chroma[2]	147	Output	L19	1.5V	LVCMOS15
Video Data Chroma[3]	149	Output	L20	1.5V	LVCMOS15
Video Data Chroma[4]	151	Output	K18	1.5V	LVCMOS15
Video Data Chroma[5]	153	Output	K19	1.5V	LVCMOS15
Video Data Chroma[6]	155	Output	J20	1.5V	LVCMOS15
Video Data Chroma[7]	157	Output	J21	1.5V	LVCMOS15
Video Data Chroma[8]	159	Output	J19	1.5V	LVCMOS15
Video Data Chroma[9]	161	Output	H19	1.5V	LVCMOS15

SPDIF Audio	27	Output	G13	1.5V	LVCMOS15
Transport Stream Clock **(27MHz)**	31	Input	H14	1.5V	LVCMOS33
Transport Stream Data Valid	33	Input	J14	1.5V	LVCMOS33
Transport Stream Data[0]	152	Input	B20	3.3V	LVCMOS33
Transport Stream Data[1]	154	Input	C19	3.3V	LVCMOS33
Transport Stream Data[2]	158	Input	A19	3.3V	LVCMOS33
Transport Stream Data[3]	160	Input	A18	3.3V	LVCMOS33
Transport Stream Data[4]	162	Input	T18	3.3V	LVCMOS33
Transport Stream Data[5]	164	Input	T20	3.3V	LVCMOS33
Transport Stream Data[6]	166	Input	T19	3.3V	LVCMOS33
Transport Stream Data[7]	**156**	Input	A20	3.3V	LVCMOS33
Uart_tx	90	Output	U18	3.3V	LVCMOS33
Uart_rx	88	Input	Y12	3.3V	LVCMOS33

3.2 Signal Formats

3.2.1 Clock Signals

When an SDI port on the PCB board is used to send out the decoded video data, the SDI clock should be connected to the **Decoder Clock** and **Use Decoder Clock** should be tied high. This will automatically synchronize the decoder outputs with the SDI interface. Internally generated clock is used if **Use Decoder Clock** is tied low.

The SDI clock frequencies are:

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60

The **Video Clock** signal is the clock for the video data output by the decoder. The frequency of the **Video clock** is determined by the video resolution, which are:

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60.

3.2.2 Video Data Signals (Output)

The output of the HD decoder FPGA Chip (for H.264 or MPEG-2) is the decoded video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma and 10 lines. And, **Video Data Chroma[0]** to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]** , **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. A **Video Clock** (refer to Section **3.2.1** for the clock frequencies) is sent out, which provides the timing for the parallel outputs of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

Output data are sampled at the rising edge of the clock. (The clock rates will correspond to the resolution and frame rate, as discussed in Section **3.2.1.)**

3.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

3.2.4 TS Stream Signals (Input)

The input of the decoder FPGA Chip is an MPEG transport stream, which is sent into the FPGA Chip by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]. Transport Stream Clock** (27MHz) is the clock for the **Transport Stream Data** lines. The **Transport Stream Data Valid** signal informs the decoder that the input is valid.

3.2.5 Decoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the decoder. **Uart_rx** receives the command from an external control device. **Uart_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Decoder API User Manual for details.

3.3 Power Supplies to the FPGA

Refer to the FPGA chip datasheet for the power supplies required. A power rail system reference design can be found in the SOC codec module datasheet, in Section **5.3 Power Rails of SoM-X-A200T** of Datasheet – MPEG Video/Audio Codec Modules– Standard Version (V.4.0, 2019)

The total power, at operation, required by a given decoder chipset ranges from 2 to 4 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails (including DDR memory), each individual power rail delivers only a portion of the total power. However, the power is not evenly distributed among the rails. Table-4 provides a power estimation for each rail for the PCB design purpose.

Table-4: Power supply estimation for the decoder chip for PCB design

Power Rail	Current (A)	Power (W)
3.3V	0.23	0.76
2.5V	0.62	1.55
1.5V	0.78	1.16
1.3V	0.23	0.30
1.2V	0.47	0.57
1.0V	2.12	2.12

Since the decoder FPGA chip normally shares the power supplies with the PCB board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 10 of this document. The reference designs provide not only the power system design and clock distributions, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: sales@soctechnologies.com for design licensing details.

3.4 Booting Sequence and Booting Time

The SOC codec IP core in the FPGA does not require special booth sequence. Refer to the FPGA data sheet for booting sequence design.

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4. The H.264 4k@30 Encoder Chipset

4.1 Pin Assignments and Pin Voltages

The chipset for H.264 encoder at 4K@30 resolution, uses the Zynq-7035 or Zynq-70345 FPGA (pin compatible). The part numbers is XC7Z035-2FFG900C and XC7Z045-2FFG900C respectively. The flash memory is S25FL128SAGNFI001 (or compatible).

In order to enable quick PCB design for the customers, SOC provides a full working design – the SOC SOM module based on the Zynq-7000 FPGAs (SOC Product Code for the module is SoM-X-Z7045). The SoM-X-Z7045 schematics (under licensing) will come with the first shipment of chipset. Information regarding the SoM-X-Z7045 and the SOC MPEG Codec modules based on the SoM-X-Z7045 can be found in:
Datasheet – MPEG Video/Audio Codecs Modules– Standard Version (V.4.0, 2019)

Table-5 lists the pin assignments and pin voltages for the H.264 4k@30 video encoder chipset based on the XC7Z045-2FFG900C (or XC7Z035-2FFG900C). The pin numbers for the SoM-X-Z7045 connected to the FPAG pins are also provided in Table-5. Refer to Appendix-C for the edge pin schematics of the SoM-X-Z7045. Further details can be found in the SoM-X-Z7045 full schematics that will be included in the first chipset shipment.

Table-5: H.264 4K@30 Encoder Chipset (based on XC7Z045-2FFG900C) **Pin Assignment and Pin Voltages**

Description	SoM-X-Z7045 Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset B	156	Input	B19	3.3V	LVCMOS33
Video Clock 0	63	Input	AC18	1.5V	LVCMOS15
Video Clock 1	80	Input	AF15	3.3V	LVCMOS33
Video Clock 2	144	Input	AE28	3.3V	LVCMOS33
Video Clock 3	105	Input	AG21	3.3V	LVCMOS33
Video Horizontal Sync	133	Input	W24	1.5V	LVCMOS15
Video Vertical Sync	113	Input	AF22	3.3V	LVCMOS33
Video Display Enable	67	Input	AD18	1.5V	LVCMOS15
Video Data 0 Luma[0]	135	Input	W25	1.5V	LVCMOS15
Video Data 0 Luma[1]	137	Input	W26	1.5V	LVCMOS15
Video Data 0 Luma[2]	116	Input	V27	1.5V	LVCMOS15
Video Data 0 Luma[3]	118	Input	W28	1.5V	LVCMOS15
Video Data 0 Luma[4]	124	Input	W29	1.5V	LVCMOS15
Video Data 0 Luma[5]	126	Input	W30	1.5V	LVCMOS15
Video Data 0 Luma[6]	128	Input	V28	1.5V	LVCMOS15
Video Data 0 Luma[7]	130	Input	V29	1.5V	LVCMOS15
Video Data 0 Luma[8]	132	Input	T30	1.5V	LVCMOS15
Video Data 0 Luma[9]	134	Input	U30	1.5V	LVCMOS15
Video Data 1 Luma[0]	117	Input	AG22	3.3V	LVCMOS33
Video Data 1 Luma[1]	119	Input	AH22	3.3V	LVCMOS33
Video Data 1 Luma[2]	121	Input	AJ21	3.3V	LVCMOS33

Video Data 1 Luma[3]	123	Input	AK21	3.3V	LVCMOS33
Video Data 1 Luma[4]	125	Input	AF23	3.3V	LVCMOS33
Video Data 1 Luma[5]	127	Input	AF24	3.3V	LVCMOS33
Video Data 1 Luma[6]	92	Input	AJ23	3.3V	LVCMOS33
Video Data 1 Luma[7]	94	Input	AJ24	3.3V	LVCMOS33
Video Data 1 Luma[8]	96	Input	AG24	3.3V	LVCMOS33
Video Data 1 Luma[9]	98	Input	AG25	3.3V	LVCMOS33
Video Data 2 Luma[0]	77	Input	AJ16	3.3V	LVCMOS33
Video Data 2 Luma[1]	79	Input	AK16	3.3V	LVCMOS33
Video Data 2 Luma[2]	81	Input	AH17	3.3V	LVCMOS33
Video Data 2 Luma[3]	83	Input	AH16	3.3V	LVCMOS33
Video Data 2 Luma[4]	85	Input	AH18	3.3V	LVCMOS33
Video Data 2 Luma[5]	87	Input	AJ18	3.3V	LVCMOS33
Video Data 2 Luma[6]	78	Input	AF13	3.3V	LVCMOS33
Video Data 2 Luma[7]	82	Input	AG15	3.3V	LVCMOS33
Video Data 2 Luma[8]	84	Input	AG17	3.3V	LVCMOS33
Video Data 2 Luma[9]	86	Input	AG16	3.3V	LVCMOS33
Video Data 3 Luma[0]	107	Input	AH21	3.3V	LVCMOS33
Video Data 3 Luma[1]	122	Input	AH29	3.3V	LVCMOS33
Video Data 3 Luma[2]	115	Input	AE22	3.3V	LVCMOS33
Video Data 3 Luma[3]	146	Input	AF28	3.3V	LVCMOS33
Video Data 3 Luma[4]	148	Input	AF29	3.3V	LVCMOS33
Video Data 3 Luma[5]	150	Input	AG29	3.3V	LVCMOS33
Video Data 3 Luma[6]	100	Input	AH23	3.3V	LVCMOS33
Video Data 3 Luma[7]	102	Input	AH24	3.3V	LVCMOS33
Video Data 3 Luma[8]	104	Input	AJ25	3.3V	LVCMOS33
Video Data 3 Luma[9]	106	Input	AK25	3.3V	LVCMOS33
Video Data 0 Chroma[0]	143	Input	T29	1.5V	LVCMOS15
Video Data 0 Chroma[1]	145	Input	U29	1.5V	LVCMOS15
Video Data 0 Chroma[2]	147	Input	R28	1.5V	LVCMOS15
Video Data 0 Chroma[3]	149	Input	T28	1.5V	LVCMOS15
Video Data 0 Chroma[4]	151	Input	P30	1.5V	LVCMOS15
Video Data 0 Chroma[5]	153	Input	R30	1.5V	LVCMOS15
Video Data 0 Chroma[6]	155	Input	N29	1.5V	LVCMOS15
Video Data 0 Chroma[7]	157	Input	P29	1.5V	LVCMOS15
Video Data 0 Chroma[8]	159	Input	N28	1.5V	LVCMOS15
Video Data 0 Chroma[9]	161	Input	P28	1.5V	LVCMOS15
Video Data 1 Chroma[0]	89	Input	AK17	3.3V	LVCMOS33
Video Data 1 Chroma[1]	91	Input	AK18	3.3V	LVCMOS33
Video Data 1 Chroma[2]	93	Input	AF19	3.3V	LVCMOS33
Video Data 1 Chroma[3]	95	Input	AG19	3.3V	LVCMOS33
Video Data 1 Chroma[4]	97	Input	AH19	3.3V	LVCMOS33
Video Data 1 Chroma[5]	99	Input	AJ19	3.3V	LVCMOS33
Video Data 1 Chroma[6]	101	Input	AF20	3.3V	LVCMOS33
Video Data 1 Chroma[7]	103	Input	AG20	3.3V	LVCMOS33
Video Data 1 Chroma[8]	109	Input	AJ20	3.3V	LVCMOS33
Video Data 1 Chroma[9]	111	Input	AK20	3.3V	LVCMOS33
Video Data 2 Chroma[0]	38	Input	AE12	3.3V	LVCMOS33

Video Data 2 Chroma[1]	40	Input	AF12	3.3V	LVCMOS33
Video Data 2 Chroma[2]	50	Input	AG12	3.3V	LVCMOS33
Video Data 2 Chroma[3]	52	Input	AH12	3.3V	LVCMOS33
Video Data 2 Chroma[4]	54	Input	AH14	3.3V	LVCMOS33
Video Data 2 Chroma[5]	56	Input	AH13	3.3V	LVCMOS33
Video Data 2 Chroma[6]	58	Input	AJ14	3.3V	LVCMOS33
Video Data 2 Chroma[7]	60	Input	AJ13	3.3V	LVCMOS33
Video Data 2 Chroma[8]	59	Input	AK13	3.3V	LVCMOS33
Video Data 2 Chroma[9]	61	Input	AK12	3.3V	LVCMOS33
Video Data 3 Chroma[0]	108	Input	AJ26	3.3V	LVCMOS33
Video Data 3 Chroma[1]	110	Input	AK26	3.3V	LVCMOS33
Video Data 3 Chroma[2]	112	Input	AH26	3.3V	LVCMOS33
Video Data 3 Chroma[3]	114	Input	AH27	3.3V	LVCMOS33
Video Data 3 Chroma[4]	136	Input	AK27	3.3V	LVCMOS33
Video Data 3 Chroma[5]	138	Input	AK28	3.3V	LVCMOS33
Video Data 3 Chroma[6]	139	Input	AJ28	3.3V	LVCMOS33
Video Data 3 Chroma[7]	141	Input	AJ29	3.3V	LVCMOS33
Video Data 3 Chroma[8]	140	Input	AJ30	3.3V	LVCMOS33
Video Data 3 Chroma[9]	142	Input	AK30	3.3V	LVCMOS33
SPDIF Audio	27	Input	Y20	1.5V	LVCMOS15
Transport Stream Buffer	29	Input	AA20	1.5V	LVCMOS15
Transport Stream Clock	31	Output	AA18	1.5V	LVCMOS15
Transport Stream Data Valid	33	Output	AA19	1.5V	LVCMOS15
Transport Stream Data [0]	152	Output	AF30	3.3V	LVCMOS33
Transport Stream Data [1]	154	Output	AG30	3.3V	LVCMOS33
Transport Stream Data [2]	158	Output	AE30	3.3V	LVCMOS33
Transport Stream Data [3]	160	Output	AB29	3.3V	LVCMOS33
Transport Stream Data [4]	162	Output	AB30	3.3V	LVCMOS33
Transport Stream Data [5]	164	Output	AA27	3.3V	LVCMOS33
Transport Stream Data [6]	166	Output	AA28	3.3V	LVCMOS33
Transport Stream Data [7]	120	Output	AH28	3.3V	LVCMOS33
Uart_tx	90	Output	AK15	3.3V	LVCMOS33
Uart_rx	88	Input	AJ15	3.3V	LVCMOS33

4.2 Signal Formats

4.2.1 Clock Signals (Input)

The 4k@30 encoder chip has 4 input clocks, **Video Clock 0**, **Video Clock 1**, **Video Clock 2**, and **Video Clock 3**. These clocks match the four of 3G SDI inputs for one 4k@30 video (assuming the 4K@30 video data are input via 4 of 3G SDI ports). However, if one of the 4k input port is used, such as HDMI 2.0 or 6 or 12G SDI, only **Video Clock 0** is needed which takes the input video clock (74.5MHz for 4k@30, and 148.5 MHz for 4k@60).

4.2.2 Video Data Signals (Input)

The input to the encoder FPGA chip is raw video data in YUV format (4:2:2 or 4:2:0), with 40 input lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma; and, 40 input lines: **Video Data 0 Chroma[0]** to **Video Data**

3 Chroma[9], for the Chroma. The precision is either 8 bits or 10 bits. For 8-bit precision, the Most Significant Luma and Chroma pins (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization if embedded SAV/EAV are not used. The video clocks (refer to Section **4.2.1**) provide the timing for the parallel input of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Video Display Enable** signal at high, when active pixels are being sent out.

The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section **4.2.1.**

4.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

4.2.4 TS stream Signals (Output)

The output of the encoder chip is MPEG Transport Stream (TS), which is sent out from the chip by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7],** along with the Transport Stream output data clock **Transport Stream Clock**. The frequency of the Transport Stream Data clock is 27MHz.

Transport Stream Buffer Ready and **Transport Stream Data Valid** are the signals to inform the user side to take over the signals.

4.2.5 Encoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the encoder. **Uart_rx** receives the command from an external control device. **Uart_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Encoder API User Manual for more details.

An external reset **PS Soft Reset_B** is available. This pin allows the user to reset the encoder when necessary. A low signal will trigger a reset. The reset signal should be maintained at high or left unconnected when in normal operation mode.

4.3 Power Supplies to the FPGA

Refer to the FPGA chip datasheet for the power supplies required. A power rail system reference design can be found in the SOC codec module datasheet, in Section **6.3 Power Rails of SoM-X-Z7045** of Datasheet – MPEG Video/Audio Codec Modules– Standard Version (V.4.0, 2019)

Since the total power is delivered over 6 power rails (including DDR memory), each individual power rail delivers only a portion of the total power. However, the power is not evenly distributed among the rails. Table-6 provides a power estimation for each rail for the encoder chip for PCB design purpose.

Table-6: Power estimation for the H.264 4k@30 encoder chipset

Power Rail	Current (A)	Power (W)
3.3V	0.31	1.02
2.5V	0.84	2.09
1.5V	0.60	0.90
1.3V	0.19	0.24
1.2V	0.15	0.18
1.0V	3.60	3.60

Since the encoder FPGA chip normally shares the power supplies with the PCB board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 10 of this document. The reference designs provide not only the power system design and clock distributions, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: sales@soctechnologies.com for design licensing details.

4.4 Booting Sequence and Booting Time

The SOC codec IP core in the FPGA does not require special booth sequence. Refer to the FPGA data sheet for booting sequence design.

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5. The H.264 4K@30 Decoder Chipset

5.1 Pin Assignments and Pin Voltages

The chipset for H.264 decoder at 4K@30 resolution, uses the Zynq-7035 or Zynq-70345 FPGA (pin compatible). The part numbers is XC7Z035-2FFG900C and XC7Z045-2FFG900C respectively. The flash memory is S25FL128SAGNFI001 (or compatible).

In order to enable quick PCB design for the customers, SOC provides a full working design – the SOC SOM module based on the Zynq-7000 FPGAs (SOC Product code of the module is SoM-X-Z7045). The SoM-X-Z7045 schematics (under licensing) will come with the first shipment of chipset. Information regarding the SoM-X-Z7045 and the SOC MPEG Codec modules based on the SoM-X-Z7045 can be found in:
Datasheet – MPEG Video/Audio Codecs Modules– Standard Version (V.4.0, 2019)

Table-7 lists the pin assignments and pin voltages for the H.264 4k@30 video decoder chipset based on the XC7Z045-2FFG900C (or XC7Z035-2FFG900C). The pin numbers for the SoM-X-Z7045 connected to the FPAG pins are also provided in Table-7. Refer to Appendix-C for the edge pin schematics of the SoM-X-Z7045. Further details can be found in the SoM-X-Z7045 full schematics that will be included in the first chipset shipment.

Table-7: 4K@30 Decoder Chip (based on XC7Z045-2FFG900C) **Pin Assignment**

Description	SoM-X-Z7045 Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset_B	156	Input	B19	3.3V	LVCMOS33
Decoder Clock	76	Input	AE13	3.3V	LVCMOS33
Video Clock	105	Output	AG21	3.3V	LVCMOS33
Video Horizontal Sync	133	Output	W24	1.5V	LVCMOS15
Video Vertical Sync	113	Output	AF22	1.5V	LVCMOS33
Video Display Enable	67	Output	AD18	1.5V	LVCMOS15
Video Data 0 Luma[0]	135	Output	W25	1.5V	LVCMOS15
Video Data 0 Luma[1]	137	Output	W26	1.5V	LVCMOS15
Video Data 0 Luma[2]	116	Output	V27	1.5V	LVCMOS15
Video Data 0 Luma[3]	118	Output	W28	1.5V	LVCMOS15
Video Data 0 Luma[4]	124	Output	W29	1.5V	LVCMOS15
Video Data 0 Luma[5]	126	Output	W30	1.5V	LVCMOS15
Video Data 0 Luma[6]	128	Output	V28	1.5V	LVCMOS15
Video Data 0 Luma[7]	130	Output	V29	1.5V	LVCMOS15
Video Data 0 Luma[8]	132	Output	T30	1.5V	LVCMOS15
Video Data 0 Luma[9]	134	Output	U30	1.5V	LVCMOS15
Video Data 1 Luma[0]	117	Output	AG22	3.3v	LVCMOS33
Video Data 1 Luma[1]	119	Output	AH22	3.3v	LVCMOS33
Video Data 1 Luma[2]	121	Output	AJ21	3.3V	LVCMOS33

Video Data 1 Luma[3]	123	Output	AK21	3.3V	LVCMOS33
Video Data 1 Luma[4]	125	Output	AF23	3.3V	LVCMOS33
Video Data 1 Luma[5]	127	Output	AF24	3.3V	LVCMOS33
Video Data 1 Luma[6]	92	Output	AJ23	3.3V	LVCMOS33
Video Data 1 Luma[7]	94	Output	AJ24	3.3V	LVCMOS33
Video Data 1 Luma[8]	96	Output	AG24	3.3V	LVCMOS33
Video Data 1 Luma[9]	98	Output	AG25	3.3V	LVCMOS33
Video Data 2 Luma[0]	77	Output	AJ16	3.3V	LVCMOS33
Video Data 2 Luma[1]	79	Output	AK16	3.3V	LVCMOS33
Video Data 2 Luma[2]	81	Output	AH17	3.3V	LVCMOS33
Video Data 2 Luma[3]	83	Output	AH16	3.3V	LVCMOS33
Video Data 2 Luma[4]	85	Output	AH18	3.3V	LVCMOS33
Video Data 2 Luma[5]	87	Output	AJ18	3.3V	LVCMOS33
Video Data 2 Luma[6]	78	Output	AF13	3.3V	LVCMOS33
Video Data 2 Luma[7]	82	Output	AG15	3.3V	LVCMOS33
Video Data 2 Luma[8]	84	Output	AG17	3.3V	LVCMOS33
Video Data 2 Luma[9]	86	Output	AG16	3.3V	LVCMOS33
Video Data 3 Luma[0]	107	Output	AH21	3.3V	LVCMOS33
Video Data 3 Luma[1]	122	Output	AH29	3.3V	LVCMOS33
Video Data 3 Luma[2]	115	Output	AE22	3.3V	LVCMOS33
Video Data 3 Luma[3]	146	Output	AF28	3.3V	LVCMOS33
Video Data 3 Luma[4]	148	Output	AF29	3.3V	LVCMOS33
Video Data 3 Luma[5]	150	Output	AG29	3.3V	LVCMOS33
Video Data 3 Luma[6]	100	Output	AH23	3.3V	LVCMOS33
Video Data 3 Luma[7]	102	Output	AH24	3.3V	LVCMOS33
Video Data 3 Luma[8]	104	Output	AJ25	3.3V	LVCMOS33
Video Data 3 Luma[9]	106	Output	AK25	3.3V	LVCMOS33
Video Data 0 Chroma[0]	143	Output	T29	1.5V	LVCMOS15
Video Data 0 Chroma[1]	145	Output	U29	1.5V	LVCMOS15
Video Data 0 Chroma[2]	147	Output	R28	1.5V	LVCMOS15
Video Data 0 Chroma[3]	149	Output	T28	1.5V	LVCMOS15
Video Data 0 Chroma[4]	151	Output	P30	1.5V	LVCMOS15
Video Data 0 Chroma[5]	153	Output	R30	1.5V	LVCMOS15
Video Data 0 Chroma[6]	155	Output	N29	1.5V	LVCMOS15
Video Data 0 Chroma[7]	157	Output	P29	1.5V	LVCMOS15
Video Data 0 Chroma[8]	159	Output	N28	1.5V	LVCMOS15
Video Data 0 Chroma[9]	161	Output	P28	1.5v	LVCMOS15
Video Data 1 Chroma[0]	89	Output	AK17	3.3V	LVCMOS33
Video Data 1 Chroma[1]	91	Output	AK18	3.3V	LVCMOS33
Video Data 1 Chroma[2]	93	Output	AF19	3.3V	LVCMOS33
Video Data 1 Chroma[3]	95	Output	AG19	3.3V	LVCMOS33
Video Data 1 Chroma[4]	97	Output	AH19	3.3V	LVCMOS33
Video Data 1 Chroma[5]	99	Output	AJ19	3.3V	LVCMOS33

Video Data 1 Chroma[6]	101	Output	AF20	3.3V	LVCMOS33
Video Data 1 Chroma[7]	103	Output	AG20	3.3V	LVCMOS33
Video Data 1 Chroma[8]	109	Output	AJ20	3.3V	LVCMOS33
Video Data 1 Chroma[9]	111	Output	AK20	3.3V	LVCMOS33
Video Data 2 Chroma[0]	38	Output	AE12	3.3V	LVCMOS33
Video Data 2 Chroma[1]	40	Output	AF12	3.3V	LVCMOS33
Video Data 2 Chroma[2]	50	Output	AG12	3.3V	LVCMOS33
Video Data 2 Chroma[3]	52	Output	AH12	3.3V	LVCMOS33
Video Data 2 Chroma[4]	54	Output	AH14	3.3V	LVCMOS33
Video Data 2 Chroma[5]	56	Output	AH13	3.3V	LVCMOS33
Video Data 2 Chroma[6]	58	Output	AJ14	3.3V	LVCMOS33
Video Data 2 Chroma[7]	60	Output	AJ13	3.3V	LVCMOS33
Video Data 2 Chroma[8]	59	Output	AK13	3.3V	LVCMOS33
Video Data 2 Chroma[9]	61	Output	AK12	3.3V	LVCMOS33
Video Data 3 Chroma[0]	108	Output	AJ26	3.3V	LVCMOS33
Video Data 3 Chroma[1]	110	Output	AK26	3.3V	LVCMOS33
Video Data 3 Chroma[2]	112	Output	AH26	3.3V	LVCMOS33
Video Data 3 Chroma[3]	114	Output	AH27	3.3V	LVCMOS33
Video Data 3 Chroma[4]	136	Output	AK27	3.3V	LVCMOS33
Video Data 3 Chroma[5]	138	Output	AK28	3.3V	LVCMOS33
Video Data 3 Chroma[6]	139	Output	AJ28	3.3V	LVCMOS33
Video Data 3 Chroma[7]	141	Output	AJ29	3.3V	LVCMOS33
Video Data 3 Chroma[8]	140	Output	AJ30	3.3V	LVCMOS33
Video Data 3 Chroma[9]	142	Output	AK30	3.3V	LVCMOS33
SPDIF Audio	27	Output	Y20	1.5V	LVCMOS15
Transport Stream Clock	31	Input	AA18	1.5V	LVCMOS15
Transport Stream Data Valid	33	input	AA19	1.5V	LVCMOS15
Transport Stream Data [0]	152	input	AF30	3.3V	LVCMOS33
Transport Stream Data [1]	154	input	AG30	3.3V	LVCMOS33
Transport Stream Data [2]	158	input	AE30	3.3V	LVCMOS33
Transport Stream Data [3]	160	input	AB29	3.3V	LVCMOS33
Transport Stream Data [4]	162	input	AB30	3.3V	LVCMOS33
Transport Stream Data [5]	164	input	AA27	3.3V	LVCMOS33
Transport Stream Data [6]	166	input	AA28	3.3V	LVCMOS33
Transport Stream Data [7]	120	input	AH28	3.3V	LVCMOS33
Uart_tx	90	Output	AK15	3.3V	LVCMOS33
Uart_rx	88	Input	AJ15	3.3V	LVCMOS33

5.2 Signal Formats

5.2.1 Video Clock Signal (Output)

The Decoder Clock signal is an input clock for driving the decoder engine. When an SDI port on the carrier board is used to send out the decoded video data, the SDI clock can be connected to the Decoder Clock. This will automatically synchronize the decoder outputs with the SDI interface.

The SDI clock frequencies are:

74.25MHz, for 4K@30

148.5MHz, for 4K@60

The **Video Clock** signal is the clock signal that provides the timing for the parallel luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The default is 148.5MHz for 4K@60 and 74.25MHz for 4K@30.

5.2.2 Video Data Signals (Output)

The output of the H.264 4k@30 decoder chip is the decoded video data in YUV format (4:2:2 or 4:2:0), with 40 output lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma; and, 40 lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision can be either 8-bit precision or 10-bit precision. For 8-bit precision, the Most Significant Bits of luma and chroma output lines (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. The Video **Display Enable signal** is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

5.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

5.2.4 Decoder Control Signals (Input and output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the decoder. **Uart_rx** receives the command from an external control device. **Uart_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Decoder API User Manual for details.

5.3 Power Supplies to the FPGA

Refer to the FPGA chip datasheet for the power supplies required. A power rail system reference design can be found in the SOC codec module datasheet, in Section **7.3 Power Rails of SoM-X-Z7045** of Datasheet – MPEG Video/Audio Codec Modules– Standard Version (V.4.0, 2019)

Since the total power is delivered over 6 power rails (including DDR memory), each individual power rail delivers only a portion of the total power. However, the power is not evenly distributed among the rails. Table-6 provides a power estimation for each rail for the carrier board PCB design purpose.

Table-8: Power estimation for the H.264 4k@30 decoder chipset

Power Rail	Current (A)	Power (W)
3.3V	0.31	1.02
2.5V	0.84	2.09
1.5V	0.60	0.90
1.3V	0.19	0.24
1.2V	0.15	0.18
1.0V	3.60	3.60

5.4 Booting Sequence and Booting Time

The SOC codec IP core in the FPGA does not require special booth sequence. Refer to the FPGA data sheet for booting sequence design. Reference design is available in the SOC **SoM-X-Z7045** schematics.

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6. The H.264 4k@60 Encoder Chipset

6.1 Pin Assignments and Pin Voltages

The chipset for H.264 encoder at 4K@60 resolution, uses the Intel Arria-10 SX660 FPGA chip. The part number is: 10AS066H4F34. The flash memory is MT25QL01GBBB8E12-0SIT (or compatible).

In order to enable quick PCB design for the customers, SOC provides a full working design of the SOC SOM module based on the 10AS066H4F34 FPGA (SOC Product Code of the module is: SoM-I-SX660). The SoM-I-SX660 schematics (under licensing) will come with the first shipment of chipset. Information regarding the SoM-I-SX660 and the SOC MPEG Codec modules based on the SoM-I-SX660 can be found in:
Datasheet – MPEG Video/Audio Codecs Modules– Standard Version (V.4.0, 2019)

Table-9 lists the pin assignments and pin voltages for the H.264 4k@60 video encoder chipset based on the 10AS066H4F34. The pin number for the SoM-I-SX660 connected to the FPAG pins are also provided in Table-9. Refer to Appendix-D for the edge pin schematics of the SoM-I-SX660. Further details can be found in the SoM-I-SX660 full schematics that will be included in the first chipset shipment.

Table-9: 4K@60 Encoder Chip (based on 10AS066H4F34) **Pin Assignment and Pin Voltages**

Description	Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
Reset In	19	Input	G18	3.3v	LVCMOS33
Video Clock 0	105	Input	AM15	3.3v	LVCMOS33
Video Clock 1	107	Input	AL15	3.3v	LVCMOS33
Video Clock 2	113	Input	E18	3.3v	LVCMOS33
Video Clock 3	115	Input	E17	3.3v	LVCMOS33
Video Data 0 Luma[0]	54	Input	AF19	3.3v	LVCMOS33
Video Data 0 Luma[1]	56	Input	AE19	3.3v	LVCMOS33
Video Data 0 Luma[2]	59	Input	AD19	3.3v	LVCMOS33
Video Data 0 Luma[3]	61	Input	AE18	3.3v	LVCMOS33
Video Data 0 Luma[4]	77	Input	AF18	3.3v	LVCMOS33
Video Data 0 Luma[5]	79	Input	AG18	3.3v	LVCMOS33
Video Data 0 Luma[6]	85	Input	AC17	3.3v	LVCMOS33
Video Data 0 Luma[7]	87	Input	AD17	3.3v	LVCMOS33
Video Data 0 Luma[8]	88	Input	AE16	3.3v	LVCMOS33
Video Data 0 Luma[9]	90	Input	AE17	3.3v	LVCMOS33
Video Data 1 Luma[0]	80	Input	AP16	3.3v	LVCMOS33
Video Data 1 Luma[1]	82	Input	AP17	3.3v	LVCMOS33
Video Data 1 Luma[2]	104	Input	AL13	3.3v	LVCMOS33
Video Data 1 Luma[3]	106	Input	AK13	3.3v	LVCMOS33
Video Data 1 Luma[4]	109	Input	AN15	3.3v	LVCMOS33
Video Data 1 Luma[5]	111	Input	AP15	3.3v	LVCMOS33
Video Data 1 Luma[6]	117	Input	AN13	3.3v	LVCMOS33
Video Data 1 Luma[7]	119	Input	AM13	3.3v	LVCMOS33

Video Data 1 Luma[8]	121	Input	AN14	3.3v	LVCMOS33
Video Data 1 Luma[9]	123	Input	AP14	3.3v	LVCMOS33
Video Data 2 Luma[0]	139	Input	F19	3.3v	LVCMOS33
Video Data 2 Luma[1]	140	Input	G20	3.3v	LVCMOS33
Video Data 2 Luma[2]	141	Input	E19	3.3v	LVCMOS33
Video Data 2 Luma[3]	142	Input	F20	3.3v	LVCMOS33
Video Data 2 Luma[4]	144	Input	K21	3.3v	LVCMOS33
Video Data 2 Luma[5]	146	Input	J21	3.3v	LVCMOS33
Video Data 2 Luma[6]	148	Input	K19	3.3v	LVCMOS33
Video Data 2 Luma[7]	150	Input	L19	3.3v	LVCMOS33
Video Data 2 Luma[8]	169	Input	F18	3.3v	LVCMOS33
Video Data 2 Luma[9]	170	Input	G21	3.3v	LVCMOS33
Video Data 3 Luma[0]	69	Input	N3	1.5v	LVCMOS15
Video Data 3 Luma[1]	131	Input	M6	1.5v	LVCMOS15
Video Data 3 Luma[2]	133	Input	M7	1.5v	LVCMOS15
Video Data 3 Luma[3]	143	Input	J4	1.5v	LVCMOS15
Video Data 3 Luma[4]	145	Input	J5	1.5v	LVCMOS15
Video Data 3 Luma[5]	147	Input	N4	1.5v	LVCMOS15
Video Data 3 Luma[6]	149	Input	N5	1.5v	LVCMOS15
Video Data 3 Luma[7]	153	Input	L5	1.5v	LVCMOS15
Video Data 3 Luma[8]	155	Input	L4	1.5v	LVCMOS15
Video Data 3 Luma[9]	157	Input	K4	1.5v	LVCMOS15
Video Data 0 Chroma[0]	50	Input	AM18	3.3v	LVCMOS33
Video Data 0 Chroma[1]	52	Input	AN18	3.3v	LVCMOS33
Video Data 0 Chroma[2]	58	Input	AK18	3.3v	LVCMOS33
Video Data 0 Chroma[3]	60	Input	AL18	3.3v	LVCMOS33
Video Data 0 Chroma[4]	76	Input	AM17	3.3v	LVCMOS33
Video Data 0 Chroma[5]	78	Input	AN17	3.3v	LVCMOS33
Video Data 0 Chroma[6]	96	Input	AL16	3.3v	LVCMOS33
Video Data 0 Chroma[7]	98	Input	AM16	3.3v	LVCMOS33
Video Data 0 Chroma[8]	101	Input	AL14	3.3v	LVCMOS33
Video Data 0 Chroma[9]	103	Input	AK14	3.3v	LVCMOS33
Video Data 1 Chroma[0]	86	Input	AH17	3.3v	LVCMOS33
Video Data 1 Chroma[1]	92	Input	AG16	3.3v	LVCMOS33
Video Data 1 Chroma[2]	81	Input	AJ17	3.3v	LVCMOS33
Video Data 1 Chroma[3]	83	Input	AK17	3.3v	LVCMOS33
Video Data 1 Chroma[4]	84	Input	AG17	3.3v	LVCMOS33
Video Data 1 Chroma[5]	89	Input	AJ16	3.3v	LVCMOS33
Video Data 1 Chroma[6]	91	Input	AK16	3.3v	LVCMOS33
Video Data 1 Chroma[7]	97	Input	AJ15	3.3v	LVCMOS33
Video Data 1 Chroma[8]	99	Input	AH15	3.3v	LVCMOS33
Video Data 1 Chroma[9]	100	Input	AJ14	3.3v	LVCMOS33
Video Data 2 Chroma[0]	93	Input	B22	3.3v	LVCMOS33
Video Data 2 Chroma[1]	95	Input	A21	3.3v	LVCMOS33
Video Data 2 Chroma[2]	108	Input	B21	3.3v	LVCMOS33
Video Data 2 Chroma[3]	110	Input	B20	3.3v	LVCMOS33
Video Data 2 Chroma[4]	112	Input	C20	3.3v	LVCMOS33
Video Data 2 Chroma[5]	114	Input	D20	3.3v	LVCMOS33

Video Data 2 Chroma[6]	120	Input	E21	3.3v	LVCMOS33
Video Data 2 Chroma[7]	122	Input	D21	3.3v	LVCMOS33
Video Data 2 Chroma[8]	136	Input	D22	3.3v	LVCMOS33
Video Data 2 Chroma[9]	138	Input	C22	3.3v	LVCMOS33
Video Data 3 Chroma[0]	116	Input	N9	1.5v	LVCMOS15
Video Data 3 Chroma[1]	118	Input	P9	1.5v	LVCMOS15
Video Data 3 Chroma[2]	124	Input	R8	1.5v	LVCMOS15
Video Data 3 Chroma[3]	126	Input	R7	1.5v	LVCMOS15
Video Data 3 Chroma[4]	128	Input	N8	1.5v	LVCMOS15
Video Data 3 Chroma[5]	130	Input	M8	1.5v	LVCMOS15
Video Data 3 Chroma[6]	132	Input	K7	1.5v	LVCMOS15
Video Data 3 Chroma[7]	134	Input	L8	1.5v	LVCMOS15
Video Data 3 Chroma[8]	135	Input	N7	1.5v	LVCMOS15
Video Data 3 Chroma[9]	137	Input	P7	1.5v	LVCMOS15
SPDIF Audio	174	Input	H20	3.3v	LVCMOS33
Transport Stream Buffer	29	Input	L1	1.5v	LVCMOS15
Transport Stream Clock	31	Output	K1	1.5v	LVCMOS15
Transport Stream Data	33	Output	K2	1.5v	LVCMOS15
Transport Stream Data [0]	46	Output	J1	1.5v	LVCMOS15
Transport Stream Data [1]	48	Output	J2	1.5v	LVCMOS15
Transport Stream Data [2]	63	Output	L3	1.5v	LVCMOS15
Transport Stream Data [3]	65	Output	K3	1.5v	LVCMOS15
Uart_tx	163	Output	H17	3.3v	LVCMOS33
Uart_rx	164	Input	J17	3.3v	LVCMOS33

6.2 Signal Formats

6.2.1 Clock Signals (Input)

The 4k@60 encoder has 4 input clocks, **Video Clock 0**, **Video Clock 1**, **Video Clock 2**, and **Video Clock 3**. These clocks match the four of 3G SDI inputs for one 4k@60 video (assuming the 4k@60 video input uses 4X3G SDI ports). However, if one 4k input is used on the carrier board, such as HDMI 2.0 or 12G SDI, only **Video Clock 0** is needed which takes the input video clock (74.5MHz for 4k@30, and 148.5 MHz for 4k@60).

6.2.2 Video Data Signals (Input)

The input to the encoder chip is raw video data in YUV format (4:2:2 or 4:2:0), with 40 input lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma; and, 40 input lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision is either 8 bits or 10 bits. For 8-bit precision, the Most Significant Luma and Chroma pins (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

The video data are sampled at both the rising and falling edges of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section **5.2.1.**

6.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

6.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 4 Dual data rate parallel lines (sampling at both the raising edge and the falling edge of the signals): **Transport Stream Data[0]** to **Transport Stream Data[4],** along with the Transport Stream output data clock **Transport Stream Clock**. The frequency of the Transport Stream Data clock is 27MHz.

For each byte of transport stream data (TS_Byte[7:0]),

at TS clock rising_edge, TS_Data[0] = TS_Byte[4], TS_Data[1] = TS_Byte[5], TS_Data[2] = TS_Byte[6], TS_Data[3] = TS_Byte[7],

at TS clock falling_edge, TS_Data[0] = TS_Byte[0], TS_Data[1] = TS_Byte[1], TS_Data[2] = TS_Byte[2], TS_Data[3] = TS_Byte[3].

Transport Stream Buffer Ready and **Transport Stream Data Valid** are the signals to inform the user side to take over the signals.

6.2.5 Encoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the encoder. **Uart_rx** receives the command from an external control device. **Uart_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Encoder API User Manual for more details.

An external reset **PS Soft Reset_B** is available. This pin allows the user to reset the encoder when necessary. A low signal will trigger a reset. The reset signal should be maintained at high or left unconnected when in normal operation mode.

6.3 Power Supplies to the FPGA

Refer to the FPGA chip datasheet for the power supplies required. A power rail system reference design can be found in the SOC codec module datasheet, in Section **8.3 Power Rails of SoM-I-SX660** of Datasheet – MPEG Video/Audio Codec Modules– Standard Version (V.4.0, 2019)

The SoM-I-SX660 (and it DDR3 chip) require the of power rails of 1.0V, 1.2V, 1.3V, 1.5V, 2.5V, and 3.3V. In the SOC SoM-I-SX660 module design, the 1.0V, 1.2V, 1.3V, 1.5V rails are created from the 2.5V, and 3.3V power rails. Table-10 provides the currents required for the two power rails, which can be used for all 4K@60 encoders and decoders.

Table-10: Power estimation for the H.264 4k@60 encoder module

Power Rail	Current (A)	Power (W)
3.3V	3.2	10.5
2.5V	1.7	4.2

Since the encoder FPGA chip normally shares the power supplies with the user PCB. The power design should be considered for both the FPGA chip and the PCB board. SOC licenses the schematics of carrier boards. The VTR-4000C discussed in Section 10 of this document is for 4k resolution. The reference design provides not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: sales@soctechnologies.com for design licensing information.

6.4 Booting Sequence and Booting Time

The SOC codec IP core in the FPGA does not require special booth sequence. However, the Arria-10 requires its booting sequence. Refer to the FPGA data sheet for booting sequence design. Reference design is available in the SOC **SoM-I-SX660** schematics. Fig. 4 shows the booting sequence used in the SoM-I-SX660 design.

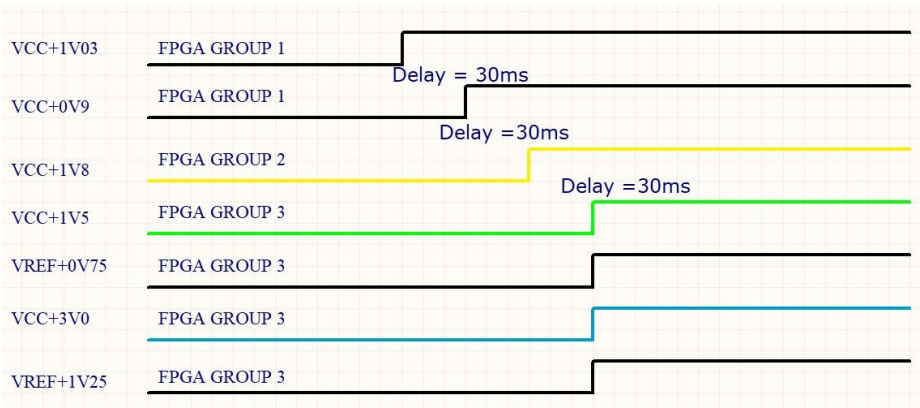

Fig. 4 Booting sequence used in the SoM-I-SX660

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7. The H.264 4K@60 Decoder Modules

7.1 Pin Assignments and Pin Voltages

The Chip for H.264 4K@60 resolution decoder use the Arria-10 SX660 (part number: 10AS066H4F34) FPGA as well. This section details the pin assignments and pin voltages for H.264 4K@60 decoder chipset based on the 10AS066H4F34 device.

Table-11 shows the pin assignments and the pin voltages for H.264 4k@60 decoder chip based on the 10AS066H4F34.

It should be noted that the 4K@60 encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

Table-11: H.264 4K@60 Decoder chip (based on 10AS066H4F34) **Pin Assignment**

Description	Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
Reset In	19	Input	G18	3.3v	LVCMOS33
Video Clock 0	100	Output	AJ14	3.3v	LVCMOS33
Video Clock 1	89	Output	AJ16	3.3v	LVCMOS33
Video Clock 2	93	Output	B22	3.3v	LVCMOS33
Video Clock 3	135	Output	N7	1.5v	LVCMOS15
Video Data 0 Luma[0]	54	Output	AF19	3.3v	LVCMOS33
Video Data 0 Luma[1]	56	Output	AE19	3.3v	LVCMOS33
Video Data 0 Luma[2]	59	Output	AD19	3.3v	LVCMOS33
Video Data 0 Luma[3]	61	Output	AE18	3.3v	LVCMOS33
Video Data 0 Luma[4]	77	Output	AF18	3.3v	LVCMOS33
Video Data 0 Luma[5]	79	Output	AG18	3.3v	LVCMOS33
Video Data 0 Luma[6]	85	Output	AC17	3.3v	LVCMOS33
Video Data 0 Luma[7]	87	Output	AD17	3.3v	LVCMOS33
Video Data 0 Luma[8]	88	Output	AE16	3.3v	LVCMOS33
Video Data 0 Luma[9]	90	Output	AE17	3.3v	LVCMOS33
Video Data 1 Luma[0]	56	Output	AP16	3.3v	LVCMOS33
Video Data 1 Luma[1]	80	Output	AP17	3.3v	LVCMOS33
Video Data 1 Luma[2]	82	Output	AL13	3.3v	LVCMOS33
Video Data 1 Luma[3]	104	Output	AK13	3.3v	LVCMOS33
Video Data 1 Luma[4]	106	Output	AN15	3.3v	LVCMOS33
Video Data 1 Luma[5]	109	Output	AP15	3.3v	LVCMOS33
Video Data 1 Luma[6]	111	Output	AN13	3.3v	LVCMOS33
Video Data 1 Luma[7]	117	Output	AM13	3.3v	LVCMOS33
Video Data 1 Luma[8]	119	Output	AN14	3.3v	LVCMOS33
Video Data 1 Luma[9]	121	Output	AP14	3.3v	LVCMOS33
Video Data 2 Luma[0]	139	Output	F19	3.3v	LVCMOS33
Video Data 2 Luma[1]	140	Output	G20	3.3v	LVCMOS33
Video Data 2 Luma[2]	141	Output	E19	3.3v	LVCMOS33
Video Data 2 Luma[3]	142	Output	F20	3.3v	LVCMOS33

Video Data 2 Luma[4]	144	Output	K21	3.3v	LVCMOS33
Video Data 2 Luma[5]	146	Output	J21	3.3v	LVCMOS33
Video Data 2 Luma[6]	148	Output	K19	3.3v	LVCMOS33
Video Data 2 Luma[7]	150	Output	L19	3.3v	LVCMOS33
Video Data 2 Luma[8]	115	Output	E17	3.3v	LVCMOS33
Video Data 2 Luma[9]	167	Output	G21	3.3v	LVCMOS33
Video Data 3 Luma[0]	69	Output	N3	1.5v	LVCMOS15
Video Data 3 Luma[1]	153	Output	L5	1.5v	LVCMOS15
Video Data 3 Luma[2]	133	Output	L6	1.5v	LVCMOS15
Video Data 3 Luma[3]	143	Output	J4	1.5v	LVCMOS15
Video Data 3 Luma[4]	145	Output	J5	1.5v	LVCMOS15
Video Data 3 Luma[5]	147	Output	N4	1.5v	LVCMOS15
Video Data 3 Luma[6]	149	Output	N5	1.5v	LVCMOS15
Video Data 3 Luma[7]	159	Output	M2	1.5v	LVCMOS15
Video Data 3 Luma[8]	155	Output	L4	1.5v	LVCMOS15
Video Data 3 Luma[9]	157	Output	K4	1.5v	LVCMOS15
Video Data 0 Chroma[0]	50	Output	AM18	3.3v	LVCMOS33
Video Data 0 Chroma[1]	52	Output	AN18	3.3v	LVCMOS33
Video Data 0 Chroma[2]	58	Output	AK18	3.3v	LVCMOS33
Video Data 0 Chroma[3]	60	Output	AL18	3.3v	LVCMOS33
Video Data 0 Chroma[4]	76	Output	AM17	3.3v	LVCMOS33
Video Data 0 Chroma[5]	78	Output	AN17	3.3v	LVCMOS33
Video Data 0 Chroma[6]	96	Output	AL16	3.3v	LVCMOS33
Video Data 0 Chroma[7]	98	Output	AM16	3.3v	LVCMOS33
Video Data 0 Chroma[8]	101	Output	AL14	3.3v	LVCMOS33
Video Data 0 Chroma[9]	103	Output	AK14	3.3v	LVCMOS33
Video Data 1 Chroma[0]	38	Output	AH18	3.3v	LVCMOS33
Video Data 1 Chroma[1]	40	Output	AH19	3.3v	LVCMOS33
Video Data 1 Chroma[2]	81	Output	AJ17	3.3v	LVCMOS33
Video Data 1 Chroma[3]	83	Output	AK17	3.3v	LVCMOS33
Video Data 1 Chroma[4]	84	Output	AG17	3.3v	LVCMOS33
Video Data 1 Chroma[5]	86	Output	AH17	3.3v	LVCMOS33
Video Data 1 Chroma[6]	91	Output	AK16	3.3v	LVCMOS33
Video Data 1 Chroma[7]	97	Output	AJ15	3.3v	LVCMOS33
Video Data 1 Chroma[8]	99	Output	AH15	3.3v	LVCMOS33
Video Data 1 Chroma[9]	105	Output	AM15	3.3v	LVCMOS33
Video Data 2 Chroma[0]	113	Output	E18	3.3v	LVCMOS33
Video Data 2 Chroma[1]	95	Output	A21	3.3v	LVCMOS33
Video Data 2 Chroma[2]	108	Output	B21	3.3v	LVCMOS33
Video Data 2 Chroma[3]	110	Output	B20	3.3v	LVCMOS33
Video Data 2 Chroma[4]	112	Output	C20	3.3v	LVCMOS33
Video Data 2 Chroma[5]	114	Output	D20	3.3v	LVCMOS33
Video Data 2 Chroma[6]	120	Output	E21	3.3v	LVCMOS33
Video Data 2 Chroma[7]	122	Output	D21	3.3v	LVCMOS33
Video Data 2 Chroma[8]	136	Output	D22	3.3v	LVCMOS33
Video Data 2 Chroma[9]	138	Output	C22	3.3v	LVCMOS33
Video Data 3 Chroma[0]	116	Output	N9	1.5v	LVCMOS15
Video Data 3 Chroma[1]	118	Output	P9	1.5v	LVCMOS15

Video Data 3 Chroma[2]	124	Output	R8	1.5v	LVCMOS15
Video Data 3 Chroma[3]	126	Output	R7	1.5v	LVCMOS15
Video Data 3 Chroma[4]	67	Output	N2	1.5v	LVCMOS15
Video Data 3 Chroma[5]	130	Output	M8	1.5v	LVCMOS15
Video Data 3 Chroma[6]	132	Output	K7	1.5v	LVCMOS15
Video Data 3 Chroma[7]	134	Output	L8	1.5v	LVCMOS15
Video Data 3 Chroma[8]	128	Output	N8	1.5v	LVCMOS15
Video Data 3 Chroma[9]	137	Output	P7	1.5v	LVCMOS15
Video Out Mode	161	Output	M3	1.5v	LVCMOS15
Video Clock in	107	Input	AL15	1.5v	LVCMOS15
SPDIF Audio	174	Output	H20	3.3v	LVCMOS33
Transport Stream Ready	29	Output	L1	1.5v	LVCMOS15
Transport Stream Data	33	Input	K2	1.5v	LVCMOS15
Transport Stream Clock in	131	Input	K6	1.5v	LVCMOS15
Transport Stream Data [0]	46	Input	J1	1.5v	LVCMOS15
Transport Stream Data [1]	48	Input	J2	1.5v	LVCMOS15
Transport Stream Data [2]	63	Input	L3	1.5v	LVCMOS15
Transport Stream Data [3]	65	Input	K3	1.5v	LVCMOS15
Uart_tx	163	Output	H17	3.3v	LVCMOS33
Uart_rx	164	Input	J17	3.3v	LVCMOS33

7.2 Signal Formats

7.2.1 Clock Signals (Output)

The 4k@60 decoder has 4 output clocks, **Video Clock 0**, **Video Clock 1**, **Video Clock 2**, and **Video Clock 3**. These clocks match the four of 3G SDI inputs for one 4k@60 video (assuming the 4k@60 video output uses 4X3G SDI ports). However, if one 4k input is used on the carrier board, such as HDMI 2.0 or 12G SDI, only **Video Clock 0** is needed which is 148.5 MHz for 4k@60).

7.2.2 Video Data Signals (Output)

The output of the H.264 4k@60 decoder module is the decoded video data in YUV format (4:2:2 or 4:2:0), with 40 output lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma; and, 40 lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision can be either 8-bit precision or 10-bit precision. For 8-bit precision, the Most Significant Bits of luma and chroma output lines (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. The Video **Display Enable signal** is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

7.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

7.2.4 TS stream Signals (Input)

The input of the decoder chip is MPEG Transport Stream (TS), which is sent into the module by 4 Dual data rate parallel lines (sampling at both the raising edge and the falling edge of the signals): **Transport Stream Data[0]** to **Transport Stream Data[4],** along with the Transport Stream input data clock **Transport Stream Clock**. The frequency of the Transport Stream Data clock is 27MHz.

For each byte of transport stream data (TS_Byte[7:0]),

at TS clock rising_edge, TS_Data[0] = TS_Byte[4], TS_Data[1] = TS_Byte[5], TS_Data[2] = TS_Byte[6], TS_Data[3] = TS_Byte[7],

at TS clock falling_edge, TS_Data[0] = TS_Byte[0], TS_Data[1] = TS_Byte[1], TS_Data[2] = TS_Byte[2], TS_Data[3] = TS_Byte[3].

Transport Stream Buffer Ready and **Transport Stream Data Valid** are the signals to inform the user side to take over the signals.

7.2.5 Decoder Control Signals (Input and output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the decoder. **Uart_rx** receives the command from an external control device. **Uart_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Decoder API User Manual for details.

7.3 Power Rails of SoM-I-SX660

The power rails for H.264 4k@60 decoder chip are the same and are also the same as the H.264 4k@60 encoder. Refer to Section 6.3 of this document for details. Table-12 provides the currents required for the two power rails, which can be used for all 4K@60 encoders and decoders.

Table-12: Power estimation for the H.264 4k@60 encoder module

Power Rail	Current (A)	Power (W)
3.3V	3.2	10.5
2.5V	1.7	4.2

Since the encoder FPGA chip normally shares the power supplies with the user PCB. The power design should be considered for both the FPGA chip and the PCB board. SOC licenses the schematics of carrier boards. The VTR-4000C discussed in Section 18 of this document is for 4k resolution. The reference design provides not only the

power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: sales@soctechnologies.com for design licensing information.

7.4 Booting Sequence and Booting Time

The SOC codec IP core in the FPGA does not require special booth sequence. However, the Arria-10 requires its booting sequence. Refer to the FPGA data sheet for booting sequence design. Reference design is available in the SOC **SoM-I-SX660** schematics. Fig. 5 shows the booting sequence used in the SoM-I-SX660 design.

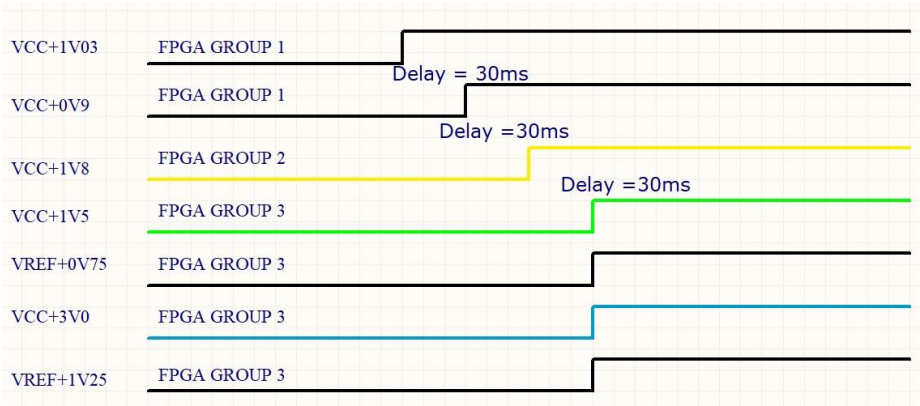

Fig. 5 Booting sequence used in the SoM-I-SX660

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8. The H.265 HD Encoder Modules

8.1 Pin Assignments and Pin Voltages

The Xilinx Zynq-7045 (part number: XC7Z045-2FFG900C) is used for H.265 HD (1080@30 or1080@60) resolution encoder chipset. This Section provides the pin assignments and electrical properties for H.265 HD encoder chip based on the XC7Z045-2FFG900C device. Table-13 lists the pin assignments and the pin voltages.

Table-13 also lists the FPGA pin numbers that are connected to the edge pins assigned to the SOC SoM-X-Z7045 module. The Zynq-7000 datasheet provides further information regarding the properties of these pins, and can be used as a reference for user PCB designs that use the XC7Z045-2FFG900C device.

Table 13: HD Encoder Chip (based on XC7Z045-2FFG900C) **Pin Assignment and Pin Voltages**

Description	SoM-X-Z7045 Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset_B	156	Input	B19	3.3V	LVCMOS33
Video Clock	105	Input	AG21	3.3V	LVCMOS33
Video Horizontal Sync	133	Input	W24	1.5V	LVCMOS15
Video Vertical Sync	113	Input	AF22	3.3V	LVCMOS33
Video Display Enable	67	Input	AD18	1.5V	LVCMOS15
Video Data Luma[0]	107	Input	AH21	3.3V	LVCMOS33
Video Data Luma[1]	122	Input	AH29	3.3V	LVCMOS33
Video Data Luma[2]	115	Input	AE22	3.3V	LVCMOS33
Video Data Luma[3]	146	Input	AF28	3.3V	LVCMOS33
Video Data Luma[4]	148	Input	AF29	3.3V	LVCMOS33
Video Data Luma[5]	150	Input	AG29	3.3V	LVCMOS33
Video Data Luma[6]	100	Input	AH23	3.3V	LVCMOS33
Video Data Luma[7]	102	Input	AH24	3.3V	LVCMOS33
Video Data Luma[8]	104	Input	AJ25	3.3V	LVCMOS33
Video Data Luma[9]	106	Input	AK25	3.3V	LVCMOS33
Video Data Chroma[0]	108	Input	AJ26	3.3V	LVCMOS33
Video Data Chroma[1]	110	Input	AK26	3.3V	LVCMOS33
Video Data Chroma[2]	112	Input	AH26	3.3V	LVCMOS33
Video Data Chroma[3]	114	Input	AH27	3.3V	LVCMOS33
Video Data Chroma[4]	136	Input	AK27	3.3V	LVCMOS33
Video Data Chroma[5]	138	Input	AK28	3.3V	LVCMOS33
Video Data Chroma[6]	139	Input	AJ28	3.3V	LVCMOS33
Video Data Chroma[7]	141	Input	AJ29	3.3V	LVCMOS33
Video Data Chroma[8]	140	Input	AJ30	3.3V	LVCMOS33
Video Data Chroma[9]	142	Input	AK30	3.3V	LVCMOS33
SPDIF Audio	27	Input	Y20	1.5V	LVCMOS15
Transport Stream Buffer Ready	29	Input	AA20	1.5V	LVCMOS15
Transport Stream Clock	31	Output	AA18	1.5V	LVCMOS15
Transport Stream Data Valid	33	Output	AA19	1.5V	LVCMOS15
Transport Stream Data[0]	152	Output	AF30	3.3V	LVCMOS33
Transport Stream Data[1]	154	Output	AG30	3.3V	LVCMOS33
Transport Stream Data[2]	158	Output	AE30	3.3V	LVCMOS33
Transport Stream Data[3]	160	Output	AB29	3.3V	LVCMOS33
Transport Stream Data[4]	162	Output	AB30	3.3V	LVCMOS33
Transport Stream Data[5]	164	Output	AA27	3.3V	LVCMOS33

Transport Stream Data[6]	166	Output	AA28	3.3V	LVCMOS33
Transport Stream Data[7]	120	Output	AH28	3.3V	LVCMOS33
Uart_tx	90	Output	AK15	3.3V	LVCMOS33
Uart_rx	88	Input	AJ15	3.3V	LVCMOS33

8.2 Signal Formats

8.2.1 Video Clock Signal (Input)

The **Video Clock** signal has two functions: (1) It is the clock for the input video data, and (2) it is the clock that drives the encoder engine.

The **Video Clock** signal usually comes from the video input interface chip, such as HDMI or SDI. It is the clock for the input video data. It is also used for driving the encoder engine. The frequency varies according to the resolution of the video input. The following are the clock frequencies for standard video resolutions.

4. 27MHz, for SD resolution
5. 74.25MHz, for 720@60 and 1080@30
6. 148.5MHz, for 1080@60

8.2.2 Video Data Signals (Input)

The input to the encoder module (H.264 or MPEG-2) is raw video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma; and, 10 input lines: **Video Data Chroma[0]** to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]** , **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization. A **Video Clock** (refer to Section **4.2.1** for the clock frequencies) is required, which provides the timing for the parallel input of luma, chroma, as well as for the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Display Enable signal** at high, when active pixels are being sent out. The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section **8.2.1.**

8.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

8.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7];** along with the Transport Stream output data clock **Transport Stream Clock.** The frequency of the Transport Stream Data clock is 27MHz.

Transport Stream Buffer Ready and **Transport Stream Data Valid** are the signals to inform the user side to take over the signals.

8.2.5 Encoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the encoder. **Uart_rx** receives the command from an external control device. **Uart_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Encoder API User Manual for more details.

An external reset PS Soft Reset_B is available. This pin allows the user to reset the encoder when necessary. A low signal will trigger a reset. The reset signal should be maintained at high or left unconnected when in normal operation mode.

8.3 Power Rails of SOM-X-Z7045

Refer to Appendix-C for the pins of power and ground on the edge connector of the SoM-X-Z7045 module.

8.4 Power Requirement and Supply Amperage

The total power, at operation, required by a given encoder chipset ranges from 2 to 10 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails, each individual power rail delivers only a portion of the total power. However, the power is not evenly distributed among the rails. Table-14 lists the power estimation, at 1080p@60 resolution, for PCB design purpose. It should be noted that the measured real power consumption is lower than the estimated power consumption, as the power estimation is for PCB design uses.

It should be noted that the power rails of 1.8v required is generated using the 2.5v power. The 6 power rails are listed in Table-14.

Table-14: Power estimation for the encoder module (1080p@60 resolution)

Power Rail	Current (A)	Power (W)
3.3V	0.37	1.22
2.5V	0.99	2.48
1.5V	1.25	1.87
1.3V	0.37	0.58

1.2V	0.75	0.90
1.0V	3.39	3.39

Since the encoder chip normally shares the power supplies with the user PCB. The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 18 of this document. The reference designs provide not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: sales@soctechnologies.com for design licensing details.

8.4 Booting Sequence and Booting Time

The SOC codec IP core in the FPGA does not require special booth sequence. Refer to the FPGA data sheet for booting sequence design. Reference design is available in the SOC **SoM-X-Z7045** schematics.

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9. The H.265 HD Decoder Chipset

9.1 Pin Assignments and Pin Voltages

The H.265 HD 1080@30 and 1080@60 decoder chips use the Xilinx Zyny-7045 FPGA, product code XC7Z045-2FFG900C. Both the H.265 HD 1080@30 and 1080@60 decoder chips have the same pin assignment.

This section details the pin assignments and pin voltages for the H.265 HD decoder chip. Table-15 shows the pin assignments and the pin voltages.

PCB designers can use the SOC SoM-X-Z7045 schematics as a design reference, which comes with first shipment of the chipset. The schematics of SoM-X-Z7045 edge connector are attached in Appendix-C of this document. Appendix-C shows the pin numbers for data, clock, control, and power, which are connected to the FPGA. It should be noted that the decoder chip uses only some of the available edge pins that are connected to the SoM-X-Z7045 module (some of the pins are not used).

It should also be noted that the HD encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module, but not on the FPGA.

Table-15: HD Decoder Module (based on SoM-X-Z7045) Pin Assignment

Description	SoM-X-Z7045 Edge Connector Pin	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset_B	156	Input	B19	3.3V	LVCMOS33
Decoder Clock	80	Input	AB13	3.3V	LVCMOS33
Video Clock	105	Output	AG21	3.3V	LVCMOS33
Video Horizontal Sync	133	Output	W24	1.5V	LVCMOS15
Video Vertical Sync	113	Output	AF22	3.3V	LVCMOS33
Video Display Enable	67	Output	AD18	1.5V	LVCMOS15
Video Data Luma[0]	107	Output	AH21	3.3V	LVCMOS33
Video Data Luma[1]	122	Output	AH29	3.3V	LVCMOS33
Video Data Luma[2]	115	Output	AE22	3.3V	LVCMOS33
Video Data Luma[3]	146	Output	AF28	3.3V	LVCMOS33
Video Data Luma[4]	148	Output	AF29	3.3V	LVCMOS33
Video Data Luma[5]	150	Output	AG29	3.3V	LVCMOS33
Video Data Luma[6]	100	Output	AH23	3.3V	LVCMOS33
Video Data Luma[7]	102	Output	AH24	3.3V	LVCMOS33
Video Data Luma[8]	104	Output	AJ25	3.3V	LVCMOS33
Video Data Luma[9]	106	Output	AK25	3.3V	LVCMOS33
Video Data Chroma[0]	108	Output	AJ26	3.3V	LVCMOS33
Video Data Chroma[1]	110	Output	AK26	3.3V	LVCMOS33
Video Data Chroma[2]	112	Output	AH26	3.3V	LVCMOS33
Video Data Chroma[3]	114	Output	AH27	3.3V	LVCMOS33
Video Data Chroma[4]	136	Output	AK27	3.3V	LVCMOS33
Video Data Chroma[5]	138	Output	AK28	3.3V	LVCMOS33
Video Data Chroma[6]	139	Output	AJ28	3.3V	LVCMOS33
Video Data Chroma[7]	141	Output	AJ29	3.3V	LVCMOS33
Video Data Chroma[8]	140	Output	AJ30	3.3V	LVCMOS33
Video Data Chroma[9]	142	Output	AK30	3.3V	LVCMOS33

SPDIF Audio	27	Output	Y20	1.5V	LVCMOS15
Transport Stream Clock **(27MHz)**	93	Input	AA18	1.5V	LVCMOS15
Transport Stream Data Valid	106	Input	AA19	1.5V	LVCMOS15
Transport Stream Data[0]	77	Input	AF30	3.3V	LVCMOS33
Transport Stream Data[1]	79	Input	AG30	3.3V	LVCMOS33
Transport Stream Data[2]	81	Input	AE30	3.3V	LVCMOS33
Transport Stream Data[3]	83	Input	AB29	3.3V	LVCMOS33
Transport Stream Data[4]	85	Input	AB30	3.3V	LVCMOS33
Transport Stream Data[5]	87	Input	AA27	3.3V	LVCMOS33
Transport Stream Data[6]	89	Input	AA28	3.3V	LVCMOS33
Transport Stream Data[7]	91	Input	AH28	3.3V	LVCMOS33
Uart_tx	90	Output	AK15	3.3V	LVCMOS33
Uart_rx	88	Input	AJ15	3.3V	LVCMOS33

9.2 Signal Formats

9.2.1 Clock Signals

When an SDI port on the PCB is used to send out the decoded video data, the SDI clock should be connected to the Decoder Clock and Use Decoder Clock should be tied high. This will automatically synchronize the decoder outputs with the SDI interface. Internally generated clock is used if Use Decoder Clock is tied low.

The SDI clock frequencies are:

8. 27MHz, for SD resolution
9. 74.25MHz, for 720@60 and 1080@30
10. 148.5MHz, for 1080@60

The **Video Clock** signal is the clock for the video data output by the decoder. The frequency of the **Video clock** is determined by the video resolution, which are:

11. 27MHz, for SD resolution
12. 74.25MHz, for 720@60 and 1080@30
13. 148.5MHz, for 1080@60.

9.2.2 Video Data Signals (Output)

The output of the HD decoder chip (H.264 or MPEG-2) is the decoded video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma and 10 lines. And, **Video Data Chroma[0]** to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]** , **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. A **Video Clock** (refer to Section **11.2.1** for the clock frequencies) is sent out, which provides the timing for the parallel inputs of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

Output data are sampled at the rising edge of the clock. (The clock rates will correspond to the resolution and frame rate, as discussed in Section **9.2.1.)**

9.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

9.2.4 TS Stream Signals (Input)

The input of the decoder module is an MPEG transport stream, which is sent into the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]. Transport Stream Clock** (27MHz) is the clock for the **Transport Stream Data** lines. The **Transport Stream Data Valid** signal informs the decoder that the input is valid.

9.2.5 Decoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the decoder. **Uart_rx** receives the command from an external control device. **Uart_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Decoder API User Manual for details.

9.4 Power Requirement and Supply Amperage

The total power, at operation, required by a given encoder chipset ranges from 2 to 7 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails, each individual power rail delivers only a portion of the total power. However, the power is not evenly distributed among the rails. Table-16 lists the power estimation, at 1080p@60 resolution, for PCB design purpose. It should be noted that the power rails of 1.8v required by the FPGA is generated using the 2.5v power.

Table-16: Power estimation for the decoder module (1080p@60 resolution)

Power Rail	Current (A)	Power (W)
3.3V	0.37	1.22
2.5V	0.99	2.48
1.5V	1.25	1.87
1.3V	0.37	0.58
1.2V	0.75	0.90
1.0V	3.39	3.39

Since the decoder FPGA (and the DDR3 memories) normally share the power supplies with the user PCB, the power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 18 of this document. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: sales@soctechnologies.com for further details.

9.4 Booting Sequence and Booting Time

The SOC codec IP core in the FPGA does not require special booth sequence. Refer to the FPGA data sheet for booting sequence design. Reference design is available in the SOC **SoM-X-Z7045** schematics.

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10. The H.265 4k@30 Encoder Modules

Note:
The "Pin Assignments and Pin Voltages" of H.265 4k@30 Encoder chip is identical to the "Pin Assignments and Pin Voltages" of H.264 4k@30 Encoder chip detailed in Section 4. However, Pin Assignments and Pin Voltages of H.265 4k@30 Encoder chip is provided here in this Section for completion.

10.1 Pin Assignments and Pin Voltages

The H.265 4k@30 encoder uses the Xilinx Zynq-7045 FPGA, product code: XC7Z045-2FFG900C. The pin assignments are the same as the H.264 4k@30 encoder module.

Table-18 lists the pin assignments and the pin voltages for the H.265 4K@30 encoder modules based on the SoM-X-Z7045.

The schematics of SoM-X-Z7045 edge connector are attached in Appendix-C of this document, which shows the pin numbers for data, clock, control, and power.

Table-18 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Zynq-7000 datasheet provides further information regarding the properties of these pins, and can be used as a reference.

Table-17: H.265 4K@30 Encoder chip (based on XC7Z045-2FFG900C) **Pin Assignment and Pin Voltages**

Description	SoM-X-Z7045 Edge	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset B	156	Input	B19	3.3V	LVCMOS33
Video Clock 0	63	Input	AC18	1.5v	LVCMOS15
Video Clock 1	80	Input	AF15	3.3v	LVCMOS33
Video Clock 2	144	Input	AE28	3.3v	LVCMOS33
Video Clock 3	105	Input	AG21	3.3v	LVCMOS33
Video Horizontal Sync	133	Input	W24	1.5v	LVCMOS15
Video Vertical Sync	113	Input	AF22	3.3v	LVCMOS33
Video Display Enable	67	Input	AD18	1.5v	LVCMOS15
Video Data 0 Luma[0]	135	Input	W25	1.5v	LVCMOS15
Video Data 0 Luma[1]	137	Input	W26	1.5v	LVCMOS15
Video Data 0 Luma[2]	116	Input	V27	1.5v	LVCMOS15
Video Data 0 Luma[3]	118	Input	W28	1.5v	LVCMOS15
Video Data 0 Luma[4]	124	Input	W29	1.5v	LVCMOS15
Video Data 0 Luma[5]	126	Input	W30	1.5v	LVCMOS15
Video Data 0 Luma[6]	128	Input	V28	1.5v	LVCMOS15
Video Data 0 Luma[7]	130	Input	V29	1.5v	LVCMOS15

Video Data 0 Luma[8]	132	Input	T30	1.5v	LVCMOS15
Video Data 0 Luma[9]	134	Input	U30	1.5v	LVCMOS15
Video Data 1 Luma[0]	117	Input	AG22	3.3v	LVCMOS33
Video Data 1 Luma[1]	119	Input	AH22	3.3v	LVCMOS33
Video Data 1 Luma[2]	121	Input	AJ21	3.3v	LVCMOS33
Video Data 1 Luma[3]	123	Input	AK21	3.3v	LVCMOS33
Video Data 1 Luma[4]	125	Input	AF23	3.3v	LVCMOS33
Video Data 1 Luma[5]	127	Input	AF24	3.3v	LVCMOS33
Video Data 1 Luma[6]	92	Input	AJ23	3.3v	LVCMOS33
Video Data 1 Luma[7]	94	Input	AJ24	3.3v	LVCMOS33
Video Data 1 Luma[8]	96	Input	AG24	3.3v	LVCMOS33
Video Data 1 Luma[9]	98	Input	AG25	3.3v	LVCMOS33
Video Data 2 Luma[0]	77	Input	AJ16	3.3v	LVCMOS33
Video Data 2 Luma[1]	79	Input	AK16	3.3v	LVCMOS33
Video Data 2 Luma[2]	81	Input	AH17	3.3v	LVCMOS33
Video Data 2 Luma[3]	83	Input	AH16	3.3v	LVCMOS33
Video Data 2 Luma[4]	85	Input	AH18	3.3v	LVCMOS33
Video Data 2 Luma[5]	87	Input	AJ18	3.3v	LVCMOS33
Video Data 2 Luma[6]	78	Input	AF13	3.3v	LVCMOS33
Video Data 2 Luma[7]	82	Input	AG15	3.3v	LVCMOS33
Video Data 2 Luma[8]	84	Input	AG17	3.3v	LVCMOS33
Video Data 2 Luma[9]	86	Input	AG16	3.3v	LVCMOS33
Video Data 3 Luma[0]	107	Input	AH21	3.3v	LVCMOS33
Video Data 3 Luma[1]	122	Input	AH29	3.3v	LVCMOS33
Video Data 3 Luma[2]	115	Input	AE22	3.3v	LVCMOS33
Video Data 3 Luma[3]	146	Input	AF28	3.3v	LVCMOS33
Video Data 3 Luma[4]	148	Input	AF29	3.3v	LVCMOS33
Video Data 3 Luma[5]	150	Input	AG29	3.3v	LVCMOS33
Video Data 3 Luma[6]	100	Input	AH23	3.3v	LVCMOS33
Video Data 3 Luma[7]	102	Input	AH24	3.3v	LVCMOS33
Video Data 3 Luma[8]	104	Input	AJ25	3.3v	LVCMOS33
Video Data 3 Luma[9]	106	Input	AK25	3.3v	LVCMOS33
Video Data 0 Chroma[0]	143	Input	T29	1.5v	LVCMOS15
Video Data 0 Chroma[1]	145	Input	U29	1.5v	LVCMOS15
Video Data 0 Chroma[2]	147	Input	R28	1.5v	LVCMOS15
Video Data 0 Chroma[3]	149	Input	T28	1.5v	LVCMOS15
Video Data 0 Chroma[4]	151	Input	P30	1.5v	LVCMOS15
Video Data 0 Chroma[5]	153	Input	R30	1.5v	LVCMOS15
Video Data 0 Chroma[6]	155	Input	N29	1.5v	LVCMOS15
Video Data 0 Chroma[7]	157	Input	P29	1.5v	LVCMOS15
Video Data 0 Chroma[8]	159	Input	N28	1.5v	LVCMOS15
Video Data 0 Chroma[9]	161	Input	P28	1.5v	LVCMOS15
Video Data 1 Chroma[0]	89	Input	AK17	3.3v	LVCMOS33
Video Data 1 Chroma[1]	91	Input	AK18	3.3v	LVCMOS33
Video Data 1 Chroma[2]	93	Input	AF19	3.3v	LVCMOS33
Video Data 1 Chroma[3]	95	Input	AG19	3.3v	LVCMOS33
Video Data 1 Chroma[4]	97	Input	AH19	3.3v	LVCMOS33
Video Data 1 Chroma[5]	99	Input	AJ19	3.3v	LVCMOS33

Video Data 1 Chroma[6]	101	Input	AF20	3.3v	LVCMOS33
Video Data 1 Chroma[7]	103	Input	AG20	3.3v	LVCMOS33
Video Data 1 Chroma[8]	109	Input	AJ20	3.3v	LVCMOS33
Video Data 1 Chroma[9]	111	Input	AK20	3.3v	LVCMOS33
Video Data 2 Chroma[0]	38	Input	AE12	3.3v	LVCMOS33
Video Data 2 Chroma[1]	40	Input	AF12	3.3v	LVCMOS33
Video Data 2 Chroma[2]	50	Input	AG12	3.3v	LVCMOS33
Video Data 2 Chroma[3]	52	Input	AH12	3.3v	LVCMOS33
Video Data 2 Chroma[4]	54	Input	AH14	3.3v	LVCMOS33
Video Data 2 Chroma[5]	56	Input	AH13	3.3v	LVCMOS33
Video Data 2 Chroma[6]	58	Input	AJ14	3.3v	LVCMOS33
Video Data 2 Chroma[7]	60	Input	AJ13	3.3v	LVCMOS33
Video Data 2 Chroma[8]	59	Input	AK13	3.3v	LVCMOS33
Video Data 2 Chroma[9]	61	Input	AK12	3.3v	LVCMOS33
Video Data 3 Chroma[0]	108	Input	AJ26	3.3v	LVCMOS33
Video Data 3 Chroma[1]	110	Input	AK26	3.3v	LVCMOS33
Video Data 3 Chroma[2]	112	Input	AH26	3.3v	LVCMOS33
Video Data 3 Chroma[3]	114	Input	AH27	3.3v	LVCMOS33
Video Data 3 Chroma[4]	136	Input	AK27	3.3v	LVCMOS33
Video Data 3 Chroma[5]	138	Input	AK28	3.3v	LVCMOS33
Video Data 3 Chroma[6]	139	Input	AJ28	3.3v	LVCMOS33
Video Data 3 Chroma[7]	141	Input	AJ29	3.3v	LVCMOS33
Video Data 3 Chroma[8]	140	Input	AJ30	3.3v	LVCMOS33
Video Data 3 Chroma[9]	142	Input	AK30	3.3v	LVCMOS33
SPDIF Audio	27	Input	Y20	1.5v	LVCMOS15
Transport Stream Buffer Ready	29	Input	AA20	1.5v	LVCMOS15
Transport Stream Clock	31	Output	AA18	1.5v	LVCMOS15
Transport Stream Data Valid	33	Output	AA19	1.5v	LVCMOS15
Transport Stream Data [0]	152	Output	AF30	3.3v	LVCMOS33
Transport Stream Data [1]	154	Output	AG30	3.3v	LVCMOS33
Transport Stream Data [2]	158	Output	AE30	3.3v	LVCMOS33
Transport Stream Data [3]	160	Output	AB29	3.3v	LVCMOS33
Transport Stream Data [4]	162	Output	AB30	3.3v	LVCMOS33
Transport Stream Data [5]	164	Output	AA27	3.3v	LVCMOS33
Transport Stream Data [6]	166	Output	AA28	3.3v	LVCMOS33
Transport Stream Data [7]	120	Output	AH28	3.3v	LVCMOS33
Uart_tx	90	Output	AK15	3.3v	LVCMOS33
Uart_rx	88	Input	AJ15	3.3v	LVCMOS33

10.2 Signal Formats

10.2.1 Clock Signals (Input)

The 4k@30 encoder chip has 4 input clocks, **Video Clock 0**, **Video Clock 1**, **Video Clock 2**, and **Video Clock 3**. These clocks match the four of 3G SDI inputs for one 4k@30/60 video (if the 4k video is input using 4X3G SID

ports). However, if one 4k input is used on the user PCB, such as HDMI 2.0 or 12G SDI, only **Video Clock 0** is needed which takes the input video clock (74.5MHz for 4k@30, and 148.5 MHz for 4k@60).

10.2.2 Video Data Signals (Input)

The input to the encoder chip is raw video data in YUV format (4:2:2 or 4:2:0), with 40 input lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma; and, 40 input lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision is either 8 bits or 10 bits. For 8-bit precision, the Most Significant Luma and Chroma pins (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization if embedded SAV/EAV are not used. The video clocks (refer to Section **10.2.1**) provide the timing for the parallel input of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Video Display Enable** signal at high, when active pixels are being sent out.

The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section **10.2.1.**

10.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

10.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7],** along with the Transport Stream output data clock **Transport Stream Clock**. The frequency of the Transport Stream Data clock is 27MHz.

Transport Stream Buffer Ready and **Transport Stream Data Valid** are the signals to inform the user side to take over the signals.

10.2.5 Encoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the encoder. **Uart_rx** receives the command from external control device. **Uart_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Encoder API User Manual for more details.

An external reset **PS Soft Reset_B** is available. This pin allows the user to reset the encoder when necessary. A low signal will trigger a reset. The reset signal should be maintained at high or left unconnected when in normal operation mode.

10.3 Power Supplies to the FPGA

Refer to the FPGA chip datasheet for the power supplies required. A power rail system reference design can be found in the SOC codec module datasheet, in Section **12.3 Power Rails of SoM-X-Z7045** of Datasheet – MPEG Video/Audio Codec Modules– Standard Version (V.4.0, 2019)

Since the total power is delivered over 6 power rails (including DDR memory), each individual power rail delivers only a portion of the total power. However, the power is not evenly distributed among the rails. Table-18 provides a power estimation for each rail for the carrier board PCB design purpose.

Table-18: Power estimation for the H.264 4k@30 encoder chipset

Power Rail	Current (A)	Power (W)
3.3V	0.50	1.63
2.5V	1.34	3.34
1.5V	0.96	1.44
1.3V	0.03	0.38
1.2V	0.24	0.29
1.0V	5.76	5.76

Since the encoder FPGA chip normally shares the power supplies with the PCB board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 18 of this document. The reference designs provide not only the power system design and clock distributions, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: sales@soctechnologies.com for design licensing details.

10.4 Booting Sequence and Booting Time

The SOC codec IP core in the FPGA does not require special booth sequence. Refer to the FPGA data sheet for booting sequence design.

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11. The H.265 4K@30 Decoder Modules

Note:
The "Pin Assignments and Pin Voltages" of H.265 4k@30 Decoder Module is identical to the "Pin Assignments and Pin Voltages" of H.264 4k@30 Decoder Module detailed in Section 7. However, Pin Assignments and Pin Voltages of H.265 4k@30 Decoder Module it is provided here in this Section for completion.

11.1 Pin Assignments and Pin Voltages

The H.265 4K@30 decoder uses the SOM-X-Z7045. The pin assignment is the same as the H.264 4K@30 decoder. This section provides again the pin assignment and pin voltages for H.265 4K@30 decoder modules based on the SoM-X-Z7045.

Table-20 shows the pin assignments and the pin voltages for H.265 4k@30 decoder modules based on the SOM-X-Z7045.

The schematics of SoM-X-Z7045 edge connector are attached in Appendix-C of this document. Appendix-C shows the pin numbers for data, clock, control, and power, which are connected to the FPGA.

It should be noted that the H.265 4K@30 encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

Table-20: 4K@30 Decoder Module (based on SoM-X-Z7045) Pin Assignment

Description	SoM-X-Z7045 Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset_B	156	Input	B19	3.3V	LVCMOS33
Video Clock	105	Output	AG21	3.3v	LVCMOS33
Video Horizontal Sync	133	Output	W24	1.5v	LVCMOS15
Video Vertical Sync	113	Output	AF22	3.3v	LVCMOS33
Video Display Enable	67	Output	AD18	1.5v	LVCMOS15
Video Data 0 Luma[0]	135	Output	W25	1.5v	LVCMOS15
Video Data 0 Luma[1]	137	Output	W26	1.5v	LVCMOS15
Video Data 0 Luma[2]	116	Output	V27	1.5v	LVCMOS15
Video Data 0 Luma[3]	118	Output	W28	1.5v	LVCMOS15
Video Data 0 Luma[4]	124	Output	W29	1.5v	LVCMOS15
Video Data 0 Luma[5]	126	Output	W30	1.5v	LVCMOS15
Video Data 0 Luma[6]	128	Output	V28	1.5v	LVCMOS15
Video Data 0 Luma[7]	130	Output	V29	1.5v	LVCMOS15
Video Data 0 Luma[8]	132	Output	T30	1.5v	LVCMOS15
Video Data 0 Luma[9]	134	Output	U30	1.5v	LVCMOS15
Video Data 1 Luma[0]	117	Output	AG22	3.3v	LVCMOS33

Video Data 1 Luma[1]	119	Output	AH22	3.3v	LVCMOS33
Video Data 1 Luma[2]	121	Output	AJ21	3.3v	LVCMOS33
Video Data 1 Luma[3]	123	Output	AK21	3.3v	LVCMOS33
Video Data 1 Luma[4]	125	Output	AF23	3.3v	LVCMOS33
Video Data 1 Luma[5]	127	Output	AF24	3.3v	LVCMOS33
Video Data 1 Luma[6]	92	Output	AJ23	3.3v	LVCMOS33
Video Data 1 Luma[7]	94	Output	AJ24	3.3v	LVCMOS33
Video Data 1 Luma[8]	96	Output	AG24	3.3v	LVCMOS33
Video Data 1 Luma[9]	98	Output	AG25	3.3v	LVCMOS33
Video Data 2 Luma[0]	77	Output	AJ16	3.3v	LVCMOS33
Video Data 2 Luma[1]	79	Output	AK16	3.3v	LVCMOS33
Video Data 2 Luma[2]	81	Output	AH17	3.3v	LVCMOS33
Video Data 2 Luma[3]	83	Output	AH16	3.3v	LVCMOS33
Video Data 2 Luma[4]	85	Output	AH18	3.3v	LVCMOS33
Video Data 2 Luma[5]	87	Output	AJ18	3.3v	LVCMOS33
Video Data 2 Luma[6]	78	Output	AF13	3.3v	LVCMOS33
Video Data 2 Luma[7]	82	Output	AG15	3.3v	LVCMOS33
Video Data 2 Luma[8]	84	Output	AG17	3.3v	LVCMOS33
Video Data 2 Luma[9]	86	Output	AG16	3.3v	LVCMOS33
Video Data 3 Luma[0]	107	Output	AH21	3.3v	LVCMOS33
Video Data 3 Luma[1]	122	Output	AH29	3.3v	LVCMOS33
Video Data 3 Luma[2]	115	Output	AE22	3.3v	LVCMOS33
Video Data 3 Luma[3]	146	Output	AF28	3.3v	LVCMOS33
Video Data 3 Luma[4]	148	Output	AF29	3.3v	LVCMOS33
Video Data 3 Luma[5]	150	Output	AG29	3.3v	LVCMOS33
Video Data 3 Luma[6]	100	Output	AH23	3.3v	LVCMOS33
Video Data 3 Luma[7]	102	Output	AH24	3.3v	LVCMOS33
Video Data 3 Luma[8]	104	Output	AJ25	3.3v	LVCMOS33
Video Data 3 Luma[9]	106	Output	AK25	3.3v	LVCMOS33
Video Data 0 Chroma[0]	143	Output	T29	1.5v	LVCMOS15
Video Data 0 Chroma[1]	145	Output	U29	1.5v	LVCMOS15
Video Data 0 Chroma[2]	147	Output	R28	1.5v	LVCMOS15
Video Data 0 Chroma[3]	149	Output	T28	1.5v	LVCMOS15
Video Data 0 Chroma[4]	151	Output	P30	1.5v	LVCMOS15
Video Data 0 Chroma[5]	153	Output	R30	1.5v	LVCMOS15
Video Data 0 Chroma[6]	155	Output	N29	1.5v	LVCMOS15
Video Data 0 Chroma[7]	157	Output	P29	1.5v	LVCMOS15
Video Data 0 Chroma[8]	159	Output	N28	1.5v	LVCMOS15
Video Data 0 Chroma[9]	161	Output	P28	1.5v	LVCMOS15
Video Data 1 Chroma[0]	89	Output	AK17	3.3v	LVCMOS33
Video Data 1 Chroma[1]	91	Output	AK18	3.3v	LVCMOS33
Video Data 1 Chroma[2]	93	Output	AF19	3.3v	LVCMOS33
Video Data 1 Chroma[3]	95	Output	AG19	3.3v	LVCMOS33

Video Data 1 Chroma[4]	97	Output	AH19	3.3v	LVCMOS33
Video Data 1 Chroma[5]	99	Output	AJ19	3.3v	LVCMOS33
Video Data 1 Chroma[6]	101	Output	AF20	3.3v	LVCMOS33
Video Data 1 Chroma[7]	103	Output	AG20	3.3v	LVCMOS33
Video Data 1 Chroma[8]	109	Output	AJ20	3.3v	LVCMOS33
Video Data 1 Chroma[9]	111	Output	AK20	3.3v	LVCMOS33
Video Data 2 Chroma[0]	38	Output	AE12	3.3v	LVCMOS33
Video Data 2 Chroma[1]	40	Output	AF12	3.3v	LVCMOS33
Video Data 2 Chroma[2]	50	Output	AG12	3.3v	LVCMOS33
Video Data 2 Chroma[3]	52	Output	AH12	3.3v	LVCMOS33
Video Data 2 Chroma[4]	54	Output	AH14	3.3v	LVCMOS33
Video Data 2 Chroma[5]	56	Output	AH13	3.3v	LVCMOS33
Video Data 2 Chroma[6]	58	Output	AJ14	3.3v	LVCMOS33
Video Data 2 Chroma[7]	60	Output	AJ13	3.3v	LVCMOS33
Video Data 2 Chroma[8]	59	Output	AK13	3.3v	LVCMOS33
Video Data 2 Chroma[9]	61	Output	AK12	3.3v	LVCMOS33
Video Data 3 Chroma[0]	108	Output	AJ26	3.3v	LVCMOS33
Video Data 3 Chroma[1]	110	Output	AK26	3.3v	LVCMOS33
Video Data 3 Chroma[2]	112	Output	AH26	3.3v	LVCMOS33
Video Data 3 Chroma[3]	114	Output	AH27	3.3v	LVCMOS33
Video Data 3 Chroma[4]	136	Output	AK27	3.3v	LVCMOS33
Video Data 3 Chroma[5]	138	Output	AK28	3.3v	LVCMOS33
Video Data 3 Chroma[6]	139	Output	AJ28	3.3v	LVCMOS33
Video Data 3 Chroma[7]	141	Output	AJ29	3.3v	LVCMOS33
Video Data 3 Chroma[8]	140	Output	AJ30	3.3v	LVCMOS33
Video Data 3 Chroma[9]	142	Output	AK30	3.3v	LVCMOS33
SPDIF Audio	27	Output	Y20	1.5v	LVCMOS15
Transport Stream Clock	31	Input	AA18	1.5v	LVCMOS15
Transport Stream Data Valid	33	input	AA19	1.5v	LVCMOS15
Transport Stream Data [0]	152	input	AF30	3.3v	LVCMOS33
Transport Stream Data [1]	154	input	AG30	3.3v	LVCMOS33
Transport Stream Data [2]	158	input	AE30	3.3v	LVCMOS33
Transport Stream Data [3]	160	input	AB29	3.3v	LVCMOS33
Transport Stream Data [4]	162	input	AB30	3.3v	LVCMOS33
Transport Stream Data [5]	164	input	AA27	3.3v	LVCMOS33
Transport Stream Data [6]	166	input	AA28	3.3v	LVCMOS33
Transport Stream Data [7]	120	input	AH28	3.3v	LVCMOS33
Uart_tx	90	Output	AK15	3.3v	LVCMOS33
Uart_rx	88	Input	AJ15	3.3v	LVCMOS33

11.2 Signal Formats

11.2.1 Video Clock Signal (Output)

The **Video Clock** signal (pin # 105) is the clock signal that provides the timing for the parallel luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The default is 148.5MHz for 4K@60 and 74.25MHz for 4K@30.

11.2.2 Video Data Signals (Output)

The output of the H.264 4k@30 decoder module is the decoded video data in YUV format (4:2:2 or 4:2:0), with 40 output lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma; and, 40 lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision can be either 8-bit precision or 10-bit precision. For 8-bit precision, the Most Significant Bits of luma and chroma output lines (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. The Video **Display Enable signal** is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

11.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

11.2.4 Decoder Control Signals (Input and output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the decoder. **Uart_rx** receives the command from an external control device. **Uart_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Decoder API User Manual for details.

11.3 Power Rails of SoM-X-Z7045

The power rails for H.265 4k@30 decoder are the same as the H.264 4k@30 decoder. Refer to Appendix-C for the pins of power and ground on the edge connector of the SoM-X-Z7045 module. However, the current required for each rail is higher.

11.4 Power Requirement and Supply Amperage

Since the total power is delivered over 6 power rails (1.0v, 1.2v, 1.3v, 1.5v, 2.5v, and 3.3v), each individual power rails deliveries only a portion of the total power. However, the power is not evenly distributed among the rails.

Table-21 lists the power estimations for each rail, at 4k@30 resolution, which can be used for PCB designs for the 4k@30 module. It should be noted that the power rails 1.8v and 2.0v are generated on the module using the input power rails. PCB designers for the carrier boards need not to consider these two rails.

Since the decoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards. The VTR-4000C, discussed in Section 18 of this document, is for 4k resolution. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: sales@soctechnologies.com for further details.

11.3 Power Supplies to the FPGA

Refer to the FPGA chip datasheet for the power supplies required. A power rail system reference design can be found in the SOC codec module datasheet, in Section **12.3 Power Rails of SoM-X-Z7045** of Datasheet – MPEG Video/Audio Codec Modules– Standard Version (V.4.0, 2019)

Since the total power is delivered over 6 power rails (including DDR memory), each individual power rail delivers only a portion of the total power. However, the power is not evenly distributed among the rails. Table-21 provides a power estimation for each rail for the carrier board PCB design purpose.

Table-21: Power estimation for the decoder chip (H.265 4K@30 resolution)

Power Rail	Current (A)	Power (W)
3.3V	0.50	1.64
2.5V	1.34	3.36
1.5V	0.96	1.44
1.3V	0.30	0.40
1.2V	0.24	0.29
1.0V	5.76	5.76

11.4 Booting Sequence and Booting Time

The SOC codec IP core in the FPGA does not require special booth sequence. Refer to the FPGA data sheet for booting sequence design.

(Left Empty here intentionally)

12. The H.265 4k@60 Encoder Chipset

To be added

13. The H.265 4k@60 Decoder Chipset

To be added

14. The H.264-to-H.265 Transcoder Chipset

By request

15. The H.264-to-MPEG2 Transcoder Chipset

By request

16. The MPEG2-to-H.264 Transcoder Chipset

By request

17. None-Standard Chipsets

By request

18. Carrier Board PCB Reference Designs

SOC has several evaluation boards for evaluating the standard encoder and decoder IP cores, modules and chipsets. These evaluation boards provide not only the DDR3 SODIMM connectors for connecting the encoder (and/or decoder) modules, but also the commonly used digital video/audio ports, such as SDI and HDMI. Ethernet port of tri-speed, 10/100/1000Mbps, as a network connection, is used in all of the SOC evaluation boards.

18.1 VTR-S1000 Evaluation Board

Fig. 6 shows a photo of the VTR-S1000 board. Major components and I/O ports are marked in the figure. Refer to the User Guide of VTR -S1000 for further details.

SOC licenses the Schematics of VTR-S1000 to the customers that have purchased the encoder (or decoder) Modules. Firmware of the VTR-S1000, including I/O drivers and network IP core, is also available for licensing. Please contact SOC sales, sales@soctechnologies.com, for details.

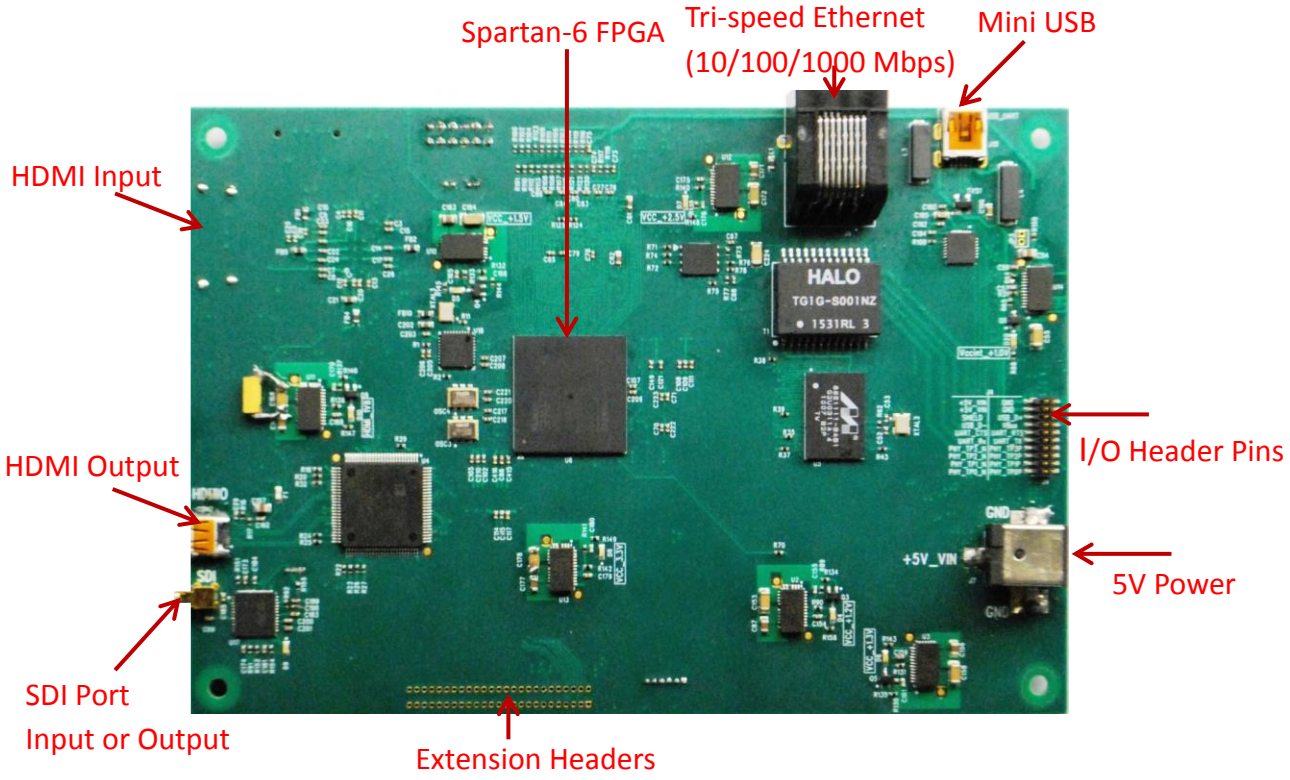

Fig. 6. FMC-MCM-1000 evaluation board

18.2 VTR-4000C Evaluation Board

Fig. 7 shows the top view of the VTR-4000C board. Major components and I/O ports are marked in the figure. Refer to the User Guide of VTR-4000C for further details.

SOC licenses the Schematics of VTR-4000C to the customers who have purchased encoder (or decoder) Modules. Firmware of the VTR-4000C, including I/O drivers and network IP core, is also available for licensing. Please contact SOC sales, sales@soctechnologies.com, for details.

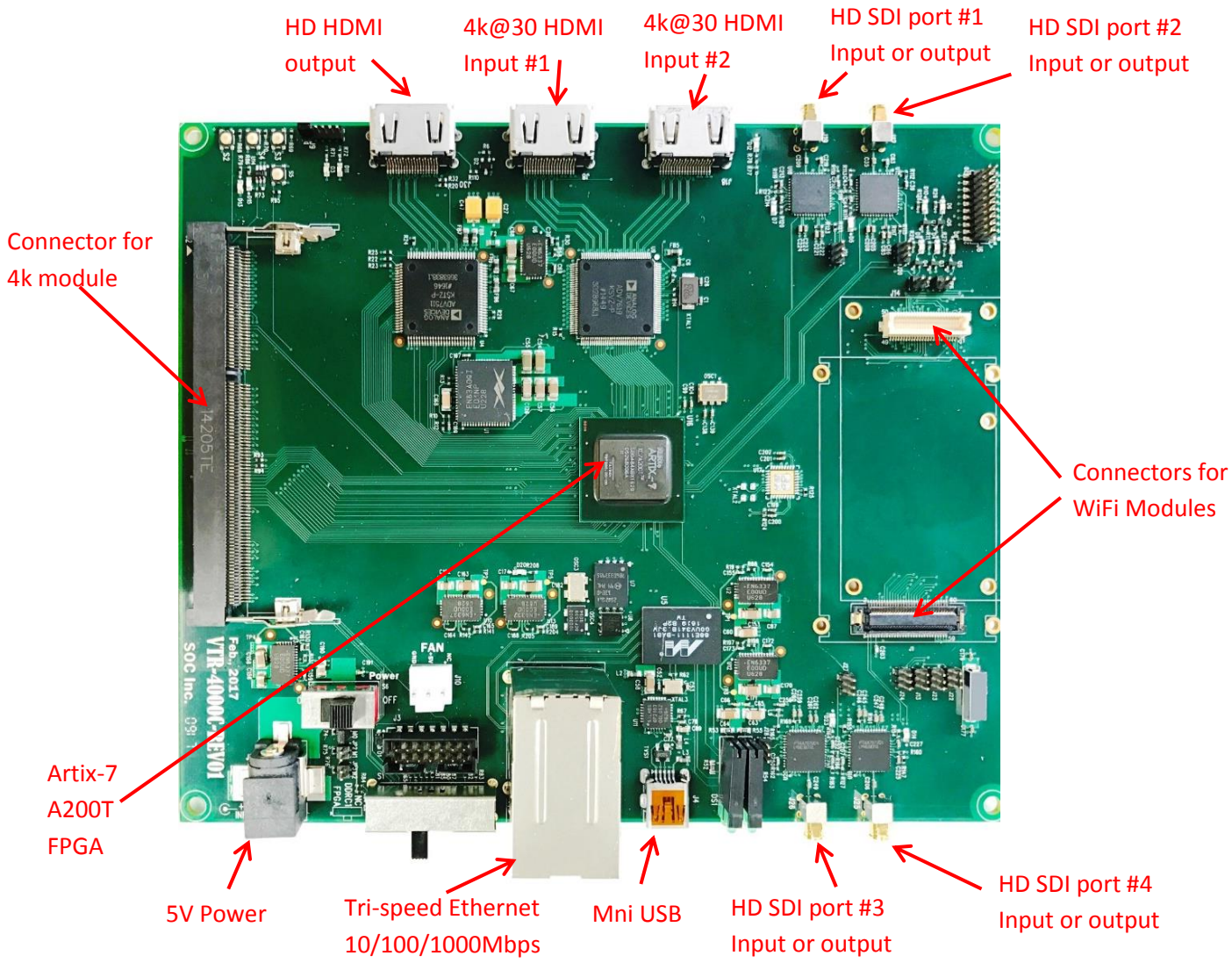

Fig. 7. VTR-4000C evaluation board top view

19. Ordering Information

The product code format has been introduced in Section 1.2, but it is shown here again in Fig. 8 for easy access. The product code for the SOC MPEG codec IP cores, modules, and chipset follows the same format.

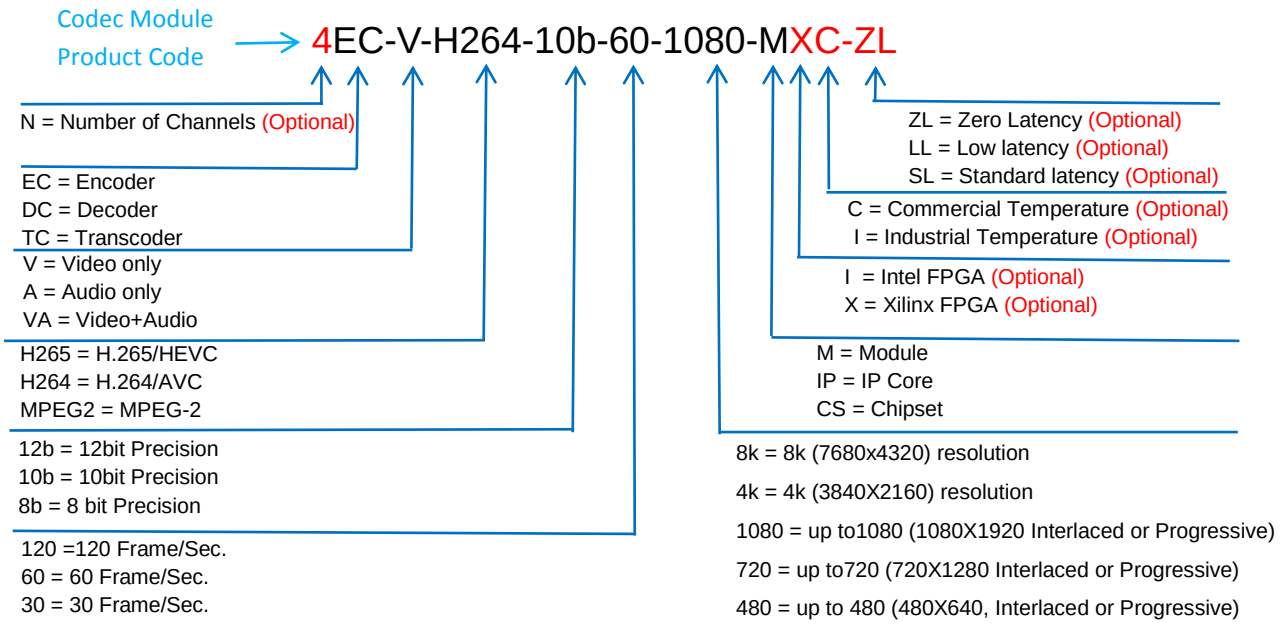

Fig. 6 SOC MPEG codec (IP cores and modules) product code naming convention

20. Contact Information

Please contact SOC head office or distributor for product details and to place an order.

Head Office

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Waterloo, ON, Canada N2V 1V9

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21. Document Revisions

Version #	Revision Date	Notes
V.1.0	10/05/2017	First release
V.1.1	19/05/2017	Minor revision
V.2.0	20/05/2017	Major revision (adding 4k)
V.3.0	10/06/2019	Major revision

Appendix-A Factory Standard Codec Chipsets

A.1 H.264 Encoder Chipsets

The H.264 encoder chipsets are based on the SOC H.264 encoder IP cores of different specifications. Table-A1 lists the product code of the factory standard video encoder chips (video only), along with the specifications for each chip. Table-A2 lists the video&audio encoder chips (both video and audio). Customers can order the encoder chipset using the product code, according to the specifications required by the application.

Table-A1: H.264 Video Encoder Chipsets:

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
EC-V-H264-8b-30-720-CS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no
EC-V-H264-8b-60-720-CS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no
EC-V-H264-8b-30-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no
EC-V-H264-10b-30-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no
EC-V-H264-8b-60-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no
EC-V-H264-10b-60-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no
EC-V-H264-8b-30-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	up to 8 bits	up to 30fps	no
EC-V-H264-10b-30-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 30fps	no
EC-V-H264-8b-60-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	8 bits	up to 60fps	no
EC-V-H264-10b-60-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	10 bits	up to 60fps	no

Table-A2: H.264 Video&Audio Encoder Chipsets:

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
EC-VA-H264-8b-30-720-CS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
EC-VA-H264-8b-60-720-CS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
EC-VA-H264-8b-30-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
EC-VA-H264-10b-30-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10bits	up to 30fps	AAC/MPEG2 L-2
EC-VA-H264-8b-60-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
EC-VA-H264-10b-60-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC/MPEG2 L-2
EC-VA-H264-8b-30-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
EC-VA-H264-10b-30-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	10 bits	up to 30fps	AAC/MPEG2 L-2
EC-VA-H264-8b-60-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
EC-VA-H264-10b-60-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	10 bits	up to 60fps	AAC/MPEG2 L-2

A.2 H.264 Decoder Chipsets

Table-A3 lists the factory standard H.264 video decoder chipsets (video only), along with the product code and specifications. Table-A4 lists the factory standard H.264 video&audio decoder chipsets, product code, and specifications.

Table-A3: H.264 Video Decoder Chipsets:

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
DC-V-H264-8b-30-720-CS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no
DC-V-H264-8b-60-720-CS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no
DC-V-H264-8b-30-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no
DC-V-H264-10b-30-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no
DC-V-H264-8b-60-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no
DC-V-H264-10b-60-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no
DC-V-H264-8b-30-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	8 bits	up to 30fps	no
DC-V-H264-10b-30-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	10 bits	up to 30fps	no
DC-V-H264-8b-60-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	8 bits	up to 60fps	no
DC-V-H264-10b-60-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	10 bits	up to 60fps	no

Table-A4: H.264 Video&Audio Decoder Chipsets:

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
DC-VA-H264-8b-30-720-CS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
DC-VA-H264-8b-60-720-CS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
DC-VA-H264-8b-30-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
DC-VA-H264-10b-30-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC/MPEG2 L-2
DC-VA-H264-8b-60-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
DC-VA-H264-10b-60-1080-CS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC/MPEG2 L-2
DC-VA-H264-8b-30-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
DC-VA-H264-10b-30-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	10 bits	up to 30fps	AAC/MPEG2 L-2
DC-VA-H264-8b-60-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
DC-VA-H264-10b-60-4k-CS	H.264	High	4k/UHD	4:2:0/4:2:2	10 bits	up to 60fps	AAC/MPEG2 L-2 L

A.1 H.265 Encoder Chipsets

The H.265 encoder chipsets are based on the SOC H.265 encoder IP cores of different configurations. Table-A5 lists the product codes of the factory standard H.265 video encoder (video only) chips, along with the specifications for each chip. Table-A6 lists the video&audio (with audio) encoder chipsets. Customers can order the H.265 encoder or video&audio chipsets using the product code, according to the specifications required by the application.

Table-A5: H.265 Video Encoder Chipsets:

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
EC-V-H265-8b-30-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no
EC-V-H265-10b-30-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no
EC-V-H265-10b-30-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 30fps	no
EC-V-H265-8b-60-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no
EC-V-H265-10b-60-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no
EC-V-H265-10b-60-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 60fps	no
EC-V-H265-8b-30-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 30fps	no
EC-V-H265-10b-30-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 30fps	no
EC-V-H265-10b-30-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12 bits	up to 30fps	no
EC-V-H265-8b-60-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 60fps	no
EC-V-H265-10b-60-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 60fps	no
EC-V-H265-10b-60-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12bits	up to 60fps	no

Note: H.265 decoder chipsets will be available in the near future.

Table-A6: H.265 Video&Audio Encoder Chipsets:

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
EC-VA-H265-8b-30-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-30-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-30-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-60-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-60-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-60-1080-CS	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-30-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-30-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-30-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-60-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-60-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-60-4k-CS	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12bits	up to 60fps	AAC or MPEG2 Layer-2

A.4 MPEG-2 Encoder Chipsets

Table-A7 lists the standard MPEG-2 video encoder chipsets. Table-A8 lists the MPEG-2 video&audio encoder chipsets. The 10-bit precision and 60 frames/second chipsets are offered as extensions of MPEG-2 standard.

Table-A7: MPEG-2 Video Encoder Chipsets:

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
EC-V-MPEG2-8b-30-720-CS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no
EC-V-MPEG2-8b-60-720-CS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no
EC-V-MPEG2-8b-30-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no
EC-V-MPEG2-10b-30-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no
EC-V-MPEG2-8b-60-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no
EC-V-MPEG2-10b-60-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no

Table-A8: MPEG-2 Video&Audio Encoder Chipsets:

Product #			Specifications				
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
EC-VA-MPEG2-8b-30-720-CS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
EC-VA-MPEG2-8b-60-720-CS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
EC-VA-MPEG2-8b-30-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
EC-VA-MPEG2-10b-30-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10bits	up to 30fps	AAC/MPEG2 L-2
EC-VA-MPEG2-8b-60-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
EC-VA-MPEG2-10b-60-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC/MPEG2 L-2

A.5 MPEG-2 Decoder Chispets

Table-A9 lists the standard MPEG-2 video decoder chipsets. Table-A10 lists the MPEG-2 video&audio decoder chipsets. The 10-bit precision and 60 frames/second chipsets are offered as extensions of MPEG-2 standard.

Table-A9: MPEG-2 Video Decoder Chipsets:

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
DC-V-MPEG2-8b-30-720-CS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no
DC-V-MPEG2-8b-60-720-CS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no
DC-V-MPEG2-8b-30-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no
DC-V-MPEG2-10b-30-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no
DC-V-MPEG2-8b-60-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no
DC-V-MPEG2-10b-60-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no

Table-A10: MPEG-2 Video&Audio Decoder Chipsets:

Product #			Specifications				
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
DC-VA-MPEG2-8b-30-720-CS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
DC-VA-MPEG2-8b-60-720-CS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
DC-VA-MPEG2-8b-30-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
DC-VA-MPEG2-10b-30-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC/MPEG2 L-2
DC-VA-MPEG2-8b-60-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
DC-VA-MPEG2-10b-60-1080-CS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC/MPEG2 L-2

A.6 H.264-to-H.265 Transcoder Chipsets

Table-A11 lists the standard H.264-to-H.265 video transcoder chipsets. Table-A12 lists the H.264-to-H.265 video&audio transcoder chipsets.

Table-A11: H.264-to-H.265 Video Transcoder Chipsets:

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Fame Rate	Audio
TC-V-H.264-to-H.265-8b-30-720-CS	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no
TC-V-H.264-to-H.265-10b-30-720-CS	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	10 bits	up to 30fps	no
TC-V- H.264-to-H.265-8b-60-720-CS	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no
TC-V- H.264-to-H.265-10b-60-720-CS	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	10 bits	up to 60fps	no
TC-V- H.264-to-H.265-8b-30-1080-CS	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no
TC-V- H.264-to-H.265-10b-30-1080-CS	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	10 bits	up to 30fps	no
TC-V- H.264-to-H.265-8b-60-1080-CS	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no
TC-V- H.264-to-H.265-10b-60-1080-CS	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	10 bits	up to 60fps	no

Table-A12: H.264-to-H.265 Video & Audio Transcoder Chipsets:

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Fame Rate	Audio
TC-V-H.264-to-H.265-8b-30-720-CS	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
TC-V-H.264-to-H.265-10b-30-720-CS	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	10 bits	up to 30fps	AAC/MPEG2 L-2
TC-V- H.264-to-H.265-8b-60-720-CS	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
TC-V- H.264-to-H.265-10b-60-720-CS	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	10 bits	up to 60fps	AAC/MPEG2 L-2
TC-V- H.264-to-H.265-8b-30-1080-CS	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2
TC-V- H.264-to-H.265-10b-30-1080-CS	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	10 bits	up to 30fps	AAC/MPEG2 L-2
TC-V- H.264-to-H.265-8b-60-1080-CS	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2
TC-V- H.264-to-H.265-10b-60-1080-CS	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	10 bits	up to 60fps	AAC/MPEG2 L-2

A.7 H.264-to-MPEG2 Transcoder Chipsets

Table-A13 lists the standard H.264-to-MPEG2 video transcoder Chipsets. Table-A14 lists the H.264-to-MPEG2 video&audio transcoder chipsets. The 60frames/second chipsets are offered as extensions of MPEG-2 standard.

Table-A13: H.264-to-MPEG2 Video Transcoder Chipsets:

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Fame Rate	Audio
TC-V-H.264-to-MPEG2-8b-30-720-CS	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no
TC-V- H.264-to-MPEG2-8b-60-720-CS	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no
TC-V- H.264-to-MPEG2-8b-30-1080-CS	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no
TC-V- H.264-to-MPEG2-8b-60-1080-CS	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no

Table-A14: H.264-to-MPEG2 Video&Audio Transcoder Chipsets:

Product #			Specifications				
	Standard	Profile	Resolution	Chroma	Precision	Fame Rate	Audio
TC-VA- H.264-to -MPEG2-8b-30-720-CS	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	AAC/MPEG2-L2
TC-VA- H.264-to -MPEG2-8b-60-720-CS	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	AAC/MPEG2-L2
TC-VA- H.264-to -MPEG2-8b-30-1080-CS	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	AAC/MPEG2-L2
TC-VA- H.264-to -MPEG2-8b-60-1080-CS	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	AAC/MPEG2-L2

A.8 MPEG2-to-H.264 Transcoder Chipsets

Table-A15 lists the standard MPEG2-to-H.264 video transcoder chipsets, and Table-A16 lists the MPEG2-to-H.264 video&audio transcoder chipsets. The 60frames/second chipsets are offered as extensions of MPEG-2 standard.

Table-A15: MPEG2-to-H.264 Video Transcoder Chipsets:

Product #			Specifications				
	Standard	Profile	Resolution	Chroma	Precision	Fame Rate	Audio
TC-V-MPEG2-to-H.264-8b-30-720-CS	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no
TC-V-MPEG2-to-H.264-8b-60-720-CS	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no
TC-V-MPEG2-to-H.264-8b-30-1080-CS	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no
TC-V-MPEG2-to-H.264-8b-60-1080-CS	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no

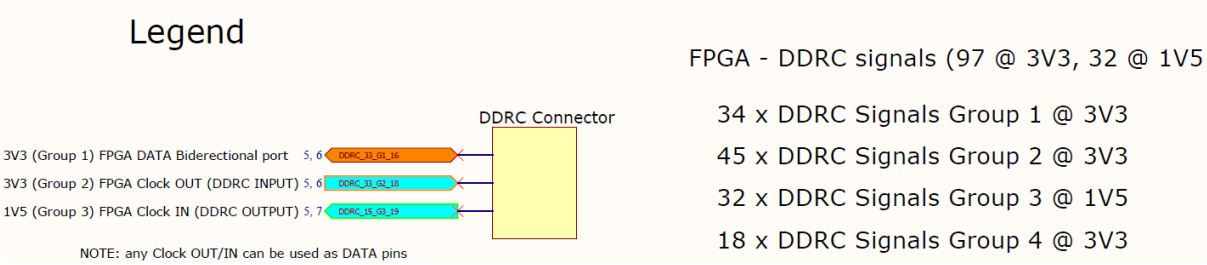
Table-A16: MPEG2-to-H.264 Video&Audio Transcoder Chipsets:

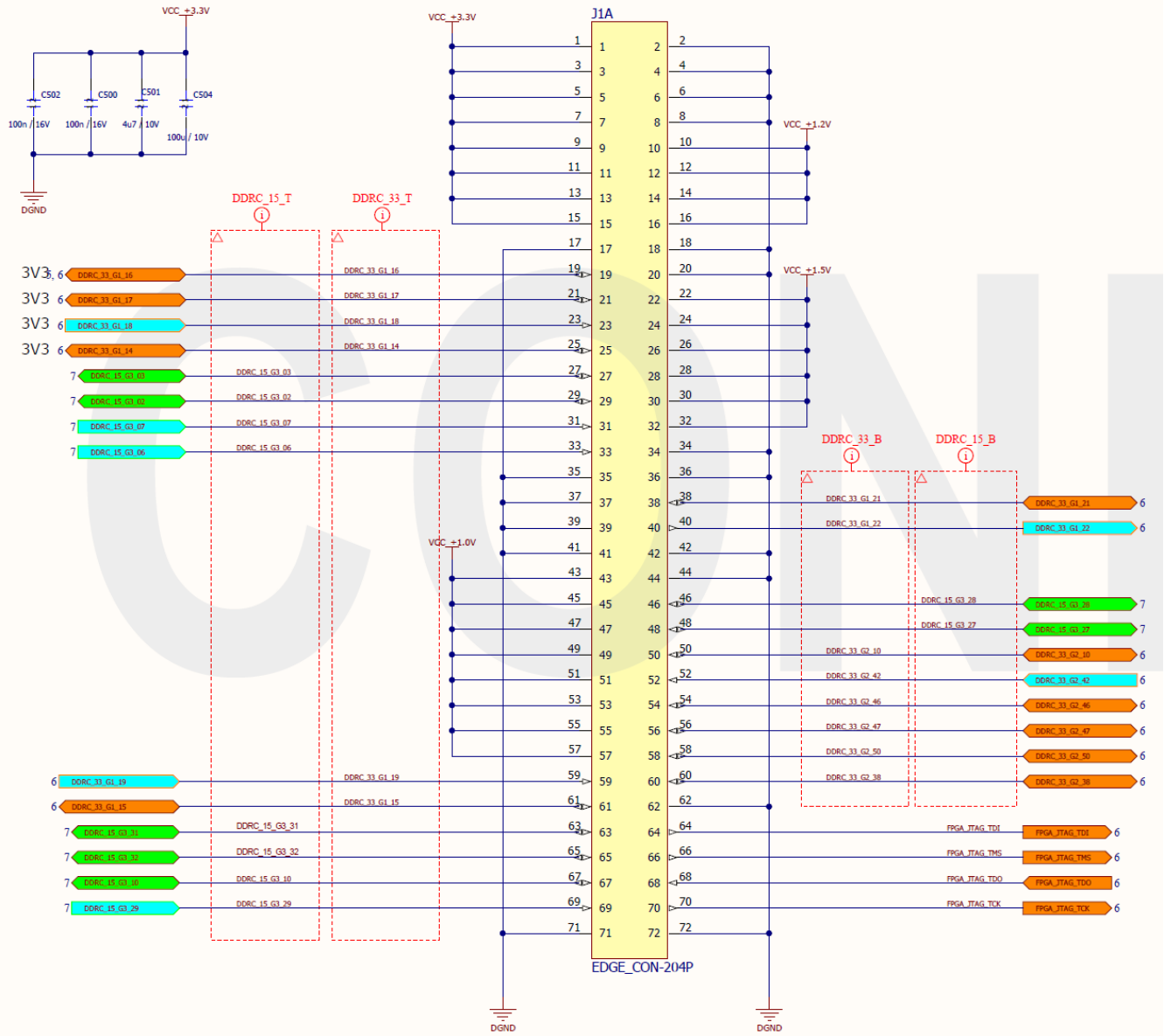
Product #			Specifications				
	Standard	Profile	Resolution	Chroma	Precision	Fame Rate	Audio
TC-VA-MPEG2-to-H.264-8b-30-720-CS	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	MPEG2-L2/AAC
TC-VA-MPEG2-to-H.264-8b-60-720-CS	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	MPEG2-L2/AAC
TC-VA-MPEG2-to-H.264-8b-30-1080-CS	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	MPEG2-L2/AAC
TC-VA-MPEG2-to-H.264-8b-60-1080-CS	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	MPEG2-L2/AAC

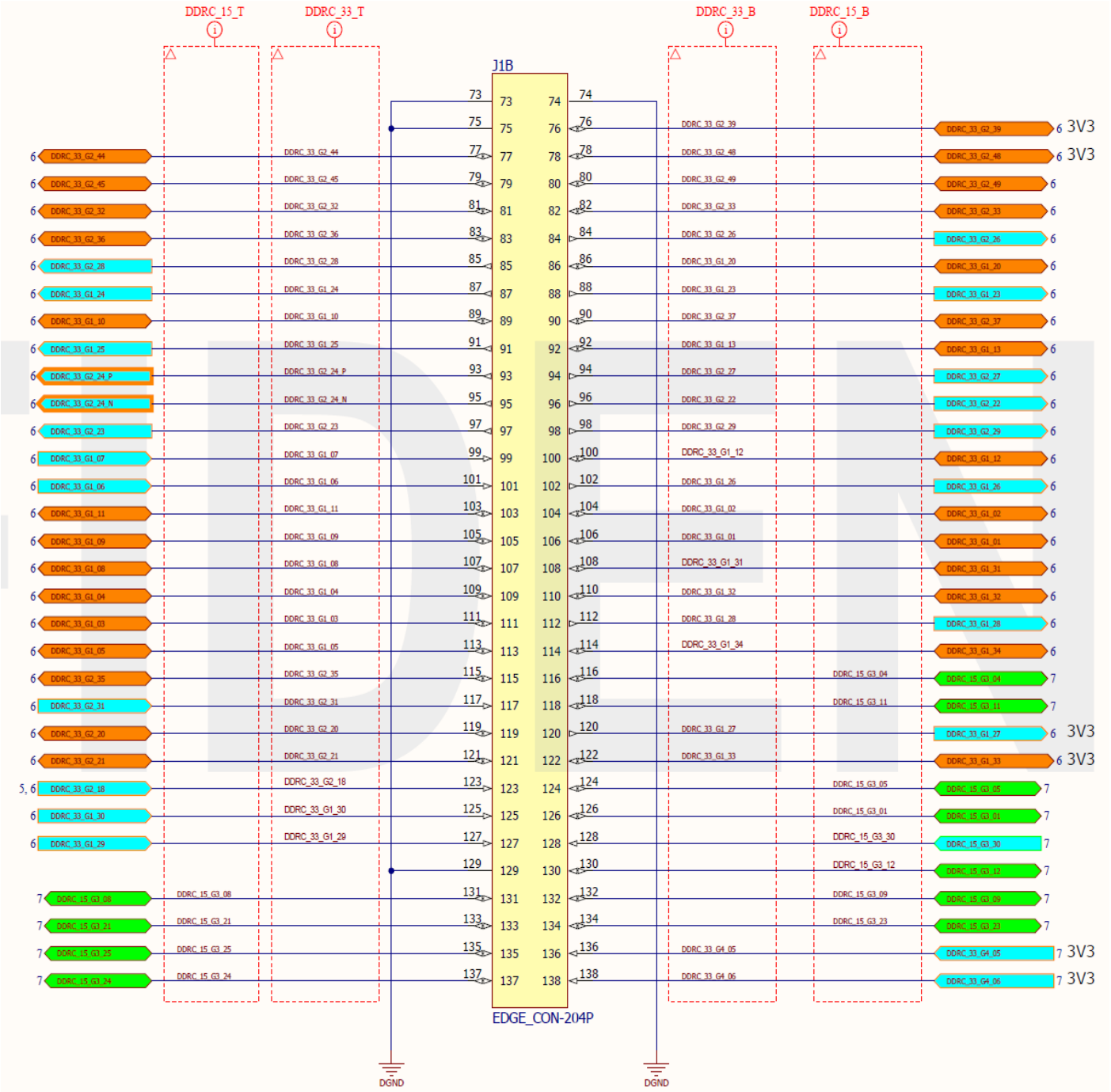
A.9 Non-Standard Codec Chipsets

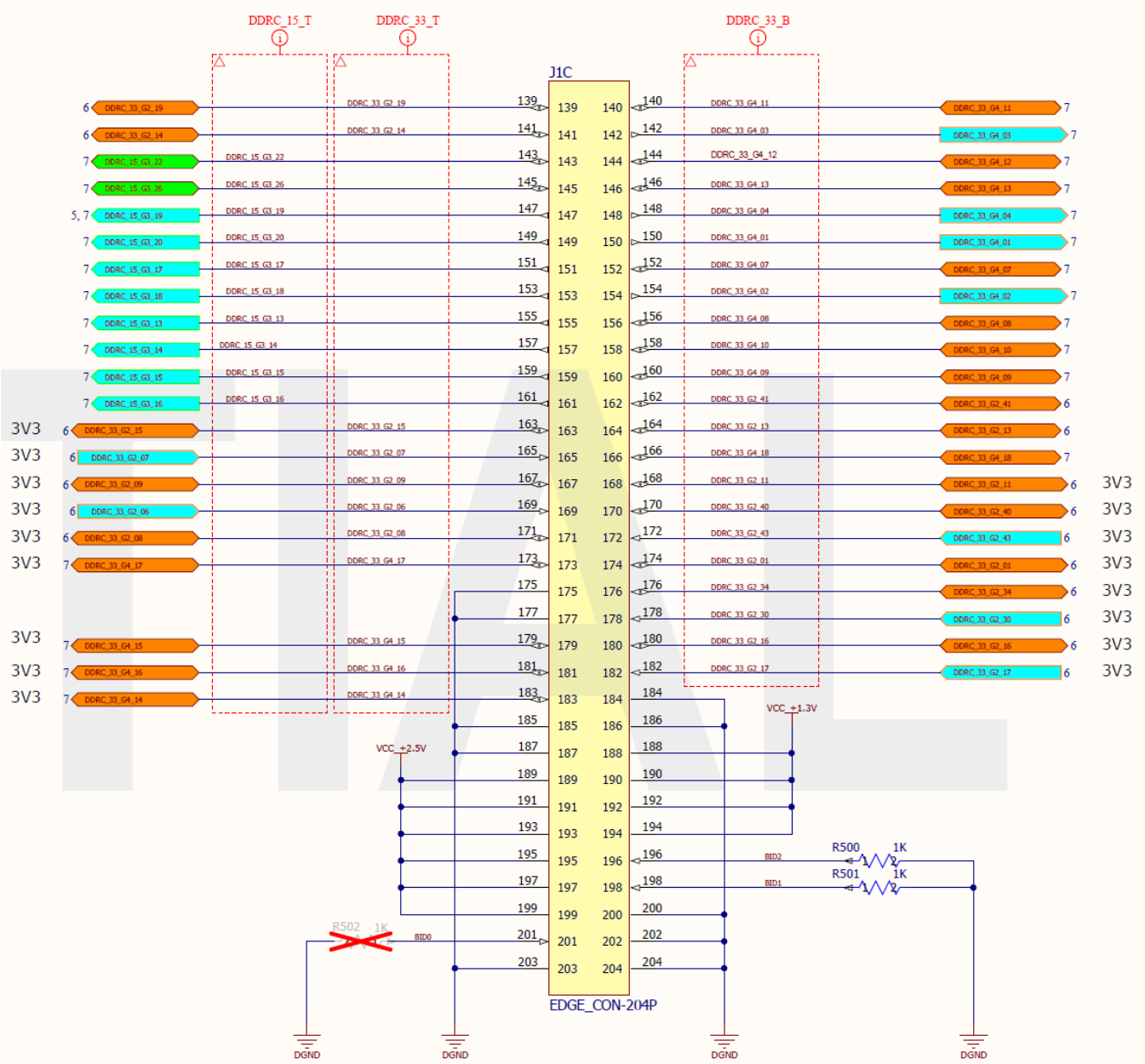
The previous sections provide the information on SOC's factory standard MPEG codec chipsets. Customers can order chipsets based on the specific requirements (non-standard chipsets). There is a Minimum Order Quantity (MOQ) or NRE required for customized configurations. Contact SOC sales sale@soctechnologies.com for more information.

Appendix - B SoM-X-A200T Edge Connector Schematics





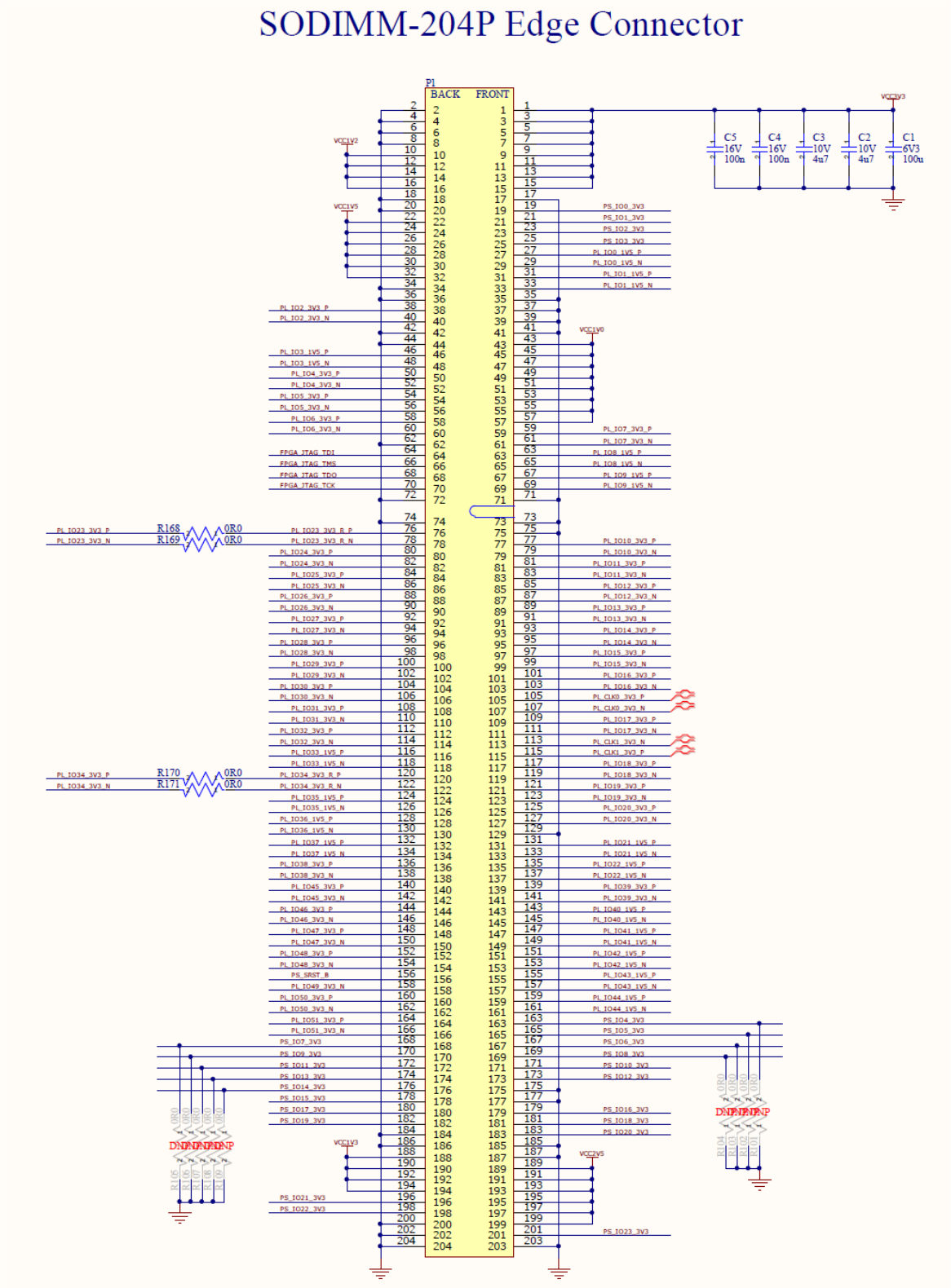

DDRC_15_T
DDRC_33_T
DDRC_33_B
DDRC_15_B
J1B
EDGE_CON-204P
DGND
DGND
3V3

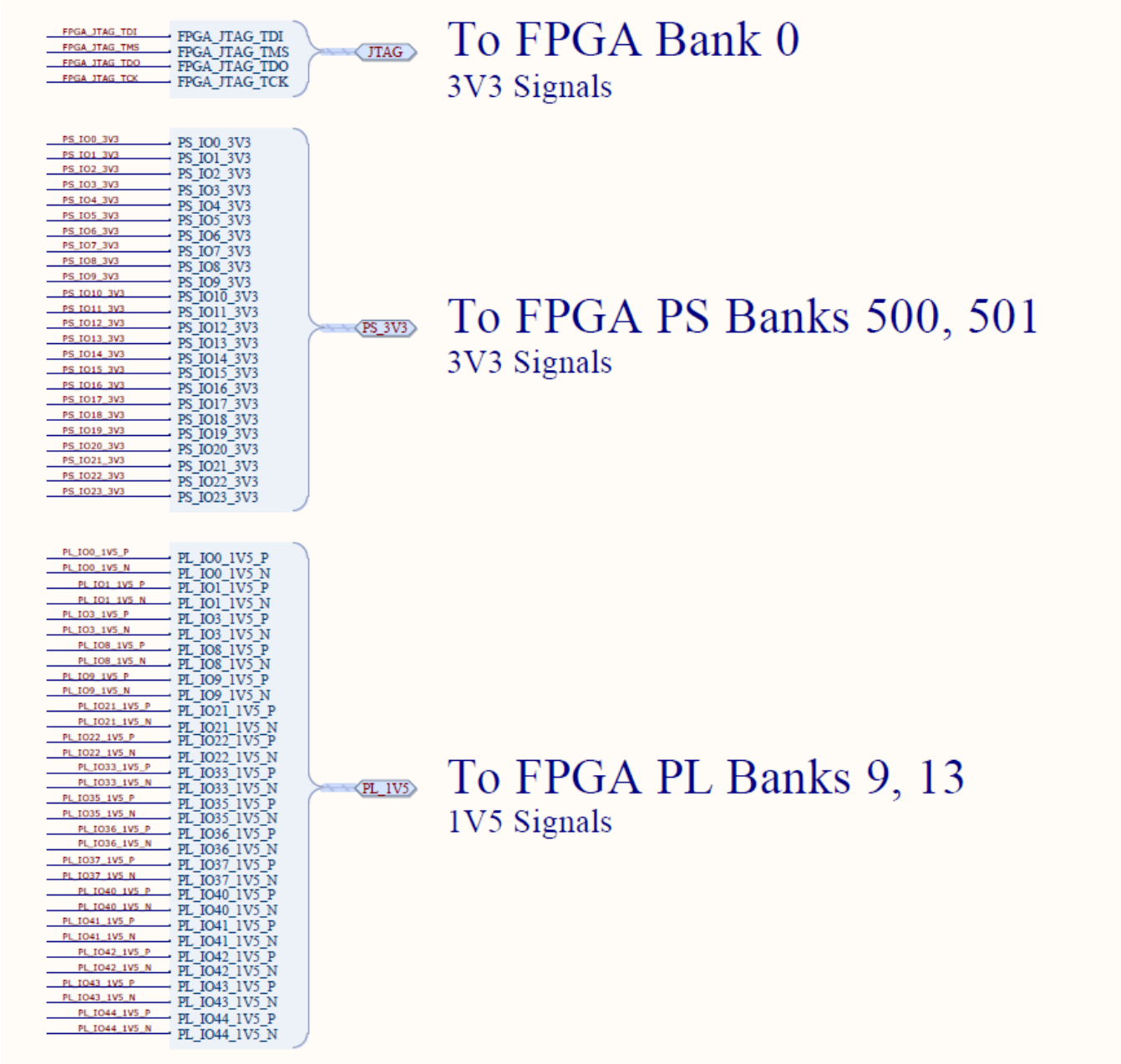


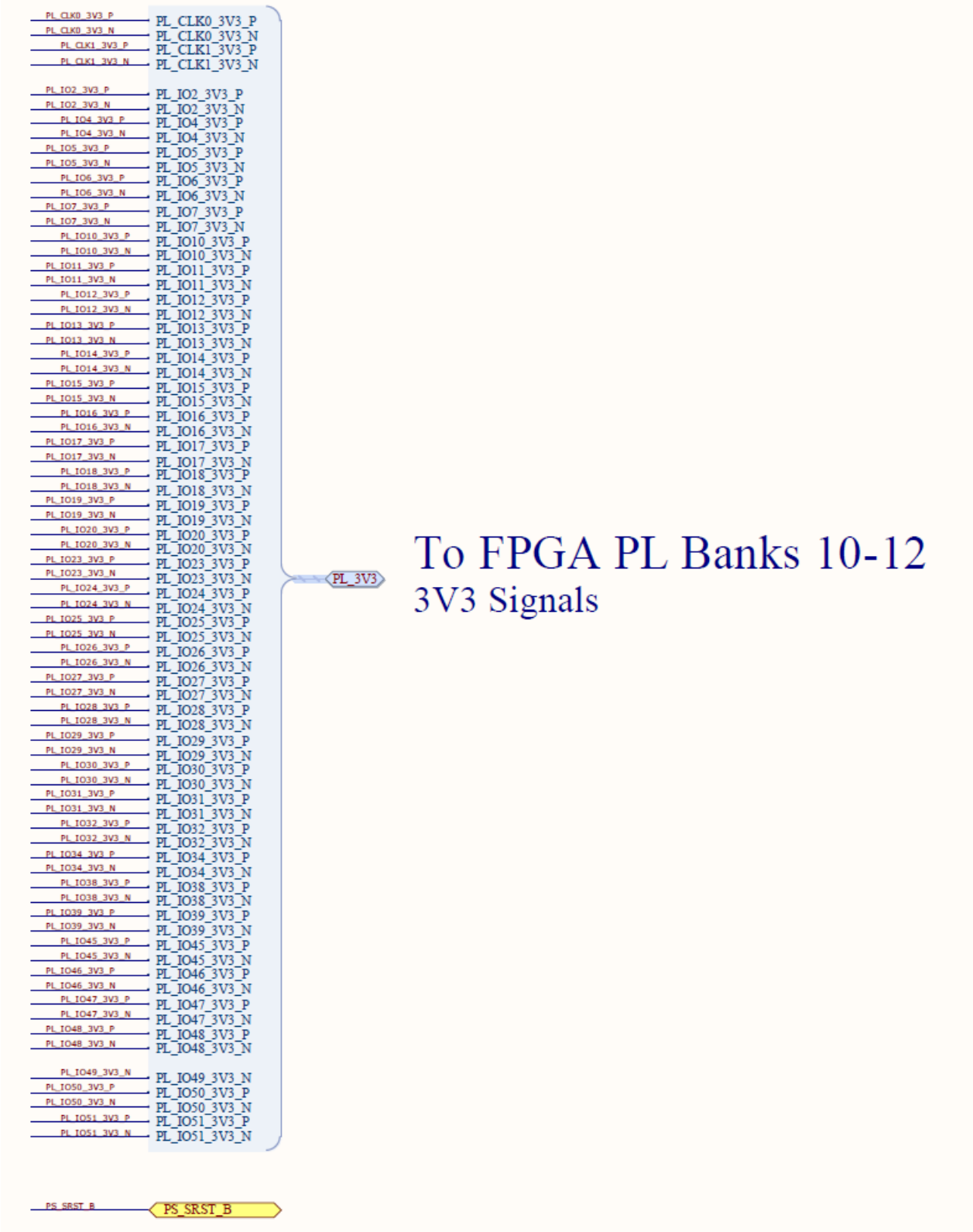
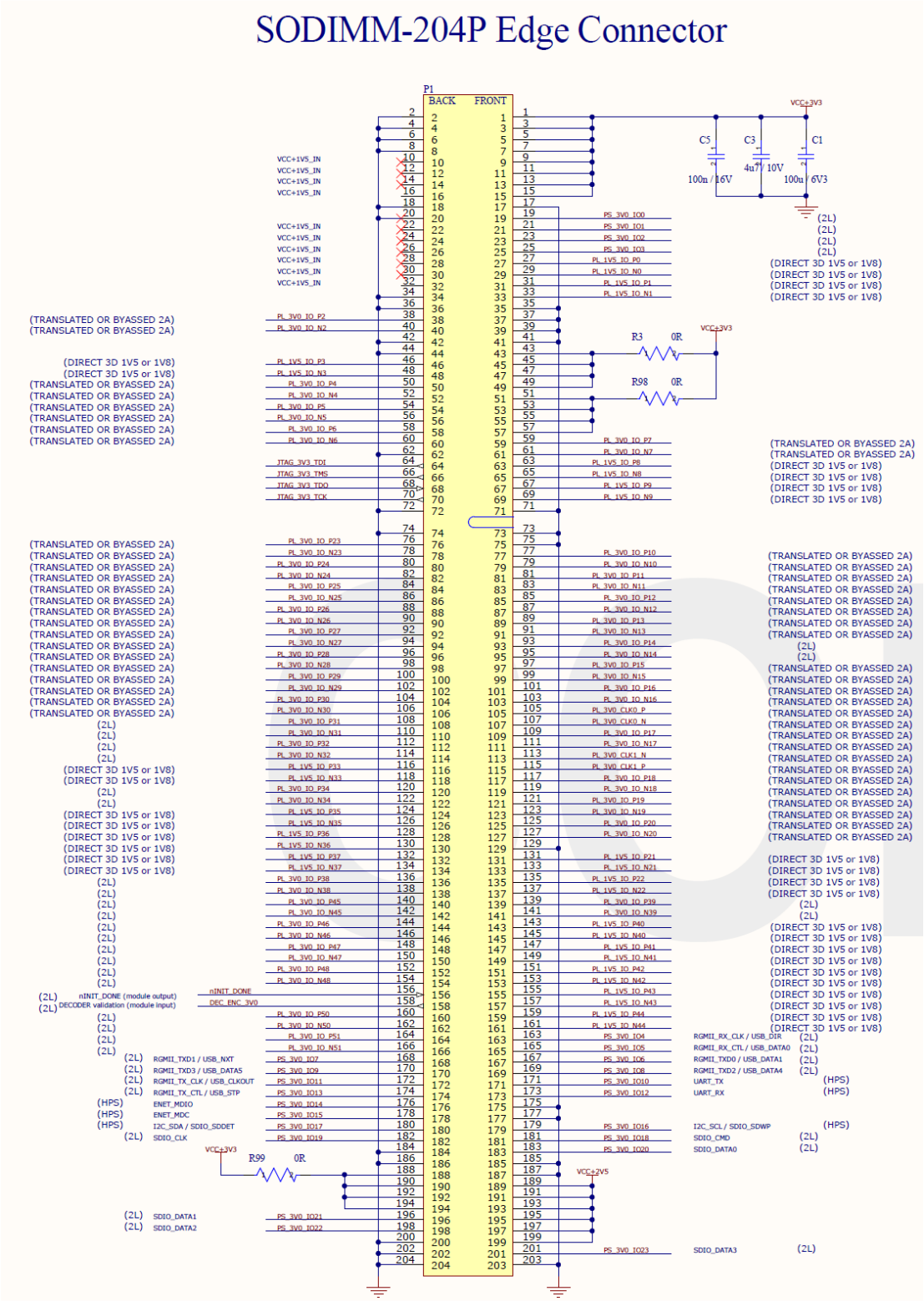
BID0	BID1	BID2	Variant
0	0	0	Standard
0	0	1	NO SDI
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

0 = POPULATED
1 = DNP
enable the pull-ups on the input pins on the carrier side

Appendix - C SoM-X-Z7045 Edge Connector Schematics




FPGA_JTAG_TDI
FPGA_JTAG_TMS
FPGA_JTAG_TDO
FPGA_JTAG_TCK
JTAG
To FPGA Bank 0
3V3 Signals
PS_IO0_3V3
PS_IO1_3V3
PS_IO2_3V3
PS_IO3_3V3
PS_IO4_3V3
PS_IO5_3V3
PS_IO6_3V3
PS_IO7_3V3
PS_IO8_3V3
PS_IO9_3V3
PS_IO10_3V3
PS_IO11_3V3
PS_IO12_3V3
PS_IO13_3V3
PS_IO14_3V3
PS_IO15_3V3
PS_IO16_3V3
PS_IO17_3V3
PS_IO18_3V3
PS_IO19_3V3
PS_IO20_3V3
PS_IO21_3V3
PS_IO22_3V3
PS_IO23_3V3
PS_3V3
To FPGA PS Banks 500, 501
3V3 Signals
PL_IO0_1V5_P
PL_IO0_1V5_N
PL_IO1_1V5_P
PL_IO1_1V5_N
PL_IO3_1V5_P
PL_IO3_1V5_N
PL_IO8_1V5_P
PL_IO8_1V5_N
PL_IO9_1V5_P
PL_IO9_1V5_N
PL_IO21_1V5_P
PL_IO21_1V5_N
PL_IO22_1V5_P
PL_IO22_1V5_N
PL_IO33_1V5_P
PL_IO33_1V5_N
PL_IO35_1V5_P
PL_IO35_1V5_N
PL_IO36_1V5_P
PL_IO36_1V5_N
PL_IO37_1V5_P
PL_IO37_1V5_N
PL_IO40_1V5_P
PL_IO40_1V5_N
PL_IO41_1V5_P
PL_IO41_1V5_N
PL_IO42_1V5_P
PL_IO42_1V5_N
PL_IO43_1V5_P
PL_IO43_1V5_N
PL_IO44_1V5_P
PL_IO44_1V5_N
PL_1V5
To FPGA PL Banks 9, 13
1V5 Signals


PL_CLK0_3V3_P
PL_CLK0_3V3_N
PL_CLK1_3V3_P
PL_CLK1_3V3_N
PL_IO2_3V3_P
PL_IO2_3V3_N
PL_IO4_3V3_P
PL_IO4_3V3_N
PL_IO5_3V3_P
PL_IO5_3V3_N
PL_IO6_3V3_P
PL_IO6_3V3_N
PL_IO7_3V3_P
PL_IO7_3V3_N
PL_IO10_3V3_P
PL_IO10_3V3_N
PL_IO11_3V3_P
PL_IO11_3V3_N
PL_IO12_3V3_P
PL_IO12_3V3_N
PL_IO13_3V3_P
PL_IO13_3V3_N
PL_IO14_3V3_P
PL_IO14_3V3_N
PL_IO15_3V3_P
PL_IO15_3V3_N
PL_IO16_3V3_P
PL_IO16_3V3_N
PL_IO17_3V3_P
PL_IO17_3V3_N
PL_IO18_3V3_P
PL_IO18_3V3_N
PL_IO19_3V3_P
PL_IO19_3V3_N
PL_IO20_3V3_P
PL_IO20_3V3_N
PL_IO23_3V3_P
PL_IO23_3V3_N
PL_IO24_3V3_P
PL_IO24_3V3_N
PL_IO25_3V3_P
PL_IO25_3V3_N
PL_IO26_3V3_P
PL_IO26_3V3_N
PL_IO27_3V3_P
PL_IO27_3V3_N
PL_IO28_3V3_P
PL_IO28_3V3_N
PL_IO29_3V3_P
PL_IO29_3V3_N
PL_IO30_3V3_P
PL_IO30_3V3_N
PL_IO31_3V3_P
PL_IO31_3V3_N
PL_IO32_3V3_P
PL_IO32_3V3_N
PL_IO34_3V3_P
PL_IO34_3V3_N
PL_IO38_3V3_P
PL_IO38_3V3_N
PL_IO39_3V3_P
PL_IO39_3V3_N
PL_IO45_3V3_P
PL_IO45_3V3_N
PL_IO46_3V3_P
PL_IO46_3V3_N
PL_IO47_3V3_P
PL_IO47_3V3_N
PL_IO48_3V3_P
PL_IO48_3V3_N
PL_IO49_3V3_N
PL_IO50_3V3_P
PL_IO50_3V3_N
PL_IO51_3V3_P
PL_IO51_3V3_N
PL_3V3
To FPGA PL Banks 10-12
3V3 Signals
PS_SRST_B
PS_SRST_B

Appendix - D SoM-I-SX660 Edge Connector Schematics