H.264 4k Video Encoder IP Core Datasheet

System-On-Chip (SOC) Technologies

1. Product Overview

The SOC H.264/AVC 4k video encoder is a single chip solution that supports single or multi-stream H.264/AVC video encoding for 4k (3840x2160) resolution, at the frame rate of 30fps, 60fps, or 120fps. The SOC 8k and 16k encoder IP cores are released as separated products.

SOC provides the versions of the H.264 4k video encoder IP core for FPGAs of both Xilinx, Altera. SOC also supplies an all-in-one 4k encoder module based on this H.264 4k video encoder IP core. Refer to the Product Brief and Datasheet for SOC MPEG codec modules for details.

The SOC H.264/AVC 4k video encoder is implemented based on SOC's proprietary single-clock driven all-hardware technology (without microprocessors or embedded software), which has significant advantages of high-speed (low latency), small footprint (low power), high video quality, and high resolution.

The SOC H.264/AVC 4k video encoder is at high profile. The encoder encodes either 4:2:0 or 4:2:2 streams whichever is desirable. The encoder has both 8-bit and 10-bit versions. The 8-bit encoder is most suited for consumer products, while the 10-bit is for high-end applications such as broadcast, digital cinema, and medical devices.

The SOC H.264/AVC 4k video encoder comes with a user API which allows the user to control the operations of the encoder, including CBR or VBR, bit rate, etc. The API user manual is shipped with the evaluation and product development kit.

The SOC encoder series can be integrated with an audio encoder to provide an all-in-one encoding solution. SOC also integrates network modules, TCP/UDP-IP, Ethernet MACs, as well as the MPEG transport multiplexer into the design to produce full system-on-chip systems. Customized versions of these products are available on request.

2. The SOC H.264/AVC Video Encoder Architecture

The SOC H.264 4k video encoder has the same architecture of HD/SD encoder. Fig. 1 is the block diagram of the SOC H.264/AVC video encoder. It is a self-contained FPGA IP core that

can be either placed into a single FPGA or integrated with other logic blocks in the same FPGA for system-on-chip solutions.

All of the blocks in the design, shown in Fig. 1, are implemented in hardware without embedded processors or embedded software, which offers high speed, low logic resource consumption, and low power. Input to the encoder is standard raw video stream in 4:2:0, 4:2:2 (or 4:4:4) format. The output of the encoder is H.264 elementary stream. SOC also provides an MPEG transport encoder to allow the output of the encoder to be in the form of MPEG transport streams.

The SOC H.264 video encoder requires two external clock sources, one at 100MHz and the second at the video clock frequency (13.5-148.5MHz). The encoder also requires an external DDR3 memory of minimum of 256MB for 1080p resolution (for both 30fps and 60fps), and 2GB for 4k resolution.

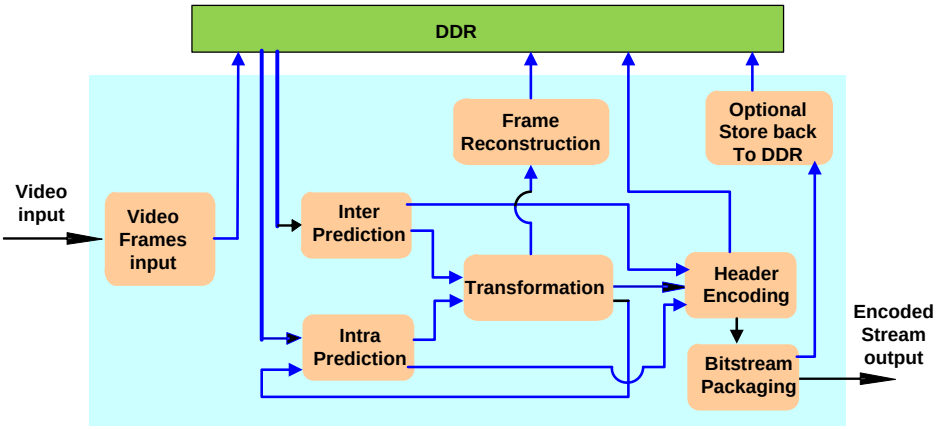

Fig. 1 Block Diagram of SOC H.264 AVC video encoder

3. Technical Specifications

Conformance Standard:
H.264/AVC (ISO/IEC14496-10)

Profiles:
The SOC H.264 video encoder supports:

- High Profile
- Main Profile
- Baseline Profile

Chroma Format:
The SOC H.264 video encoder supports:
- 4:2:0
- 4:2:2
- 4:4:4 (on request)

Precision:
- 8 bits
- 10 bits.

Frame Rate:
The SOC H.264 video encoder supports:
- 10fps
- 24fps
- 25fps
- 29.97fps
- 30fps
- 60fps
- 120fps
- Higher frame rates are also available, on request

Inter Frames:
The SOC H.264 video encoder supports:
- I frame
- P frame
- B frame (available, but not recommended)

Latency:
The SOC H.264 video encoder has very low latency due to its hardware implementation. The encoding engine latency is less 0.5ms from data in to data out. The encoder can buffer 1 complete frame before encoding to compensate any jitters of the input stream, when necessary.

Bit Rate:
- Constant Bit Rate – User controllable through API
- Variable Bit Rate – User controllable through API.

Power:
The power consumption is less than 1.5w for core only for 4k resolution.

4. Targeted FPGAs and Logic Resources

The SOC H.264 4k video encoder IP core is customized for both Xilinx and Altera FPGAs, including:

- Kitex-7
- Zynq-7
- Ultrascale
- Arria-10
- Stratix-V

Logic Resources on Xilinx FPGAs:

The logic resources required on Xilinx FPGAs by the 4k@30/60/120 encoder IP core is listed in Table-1

Resources type	4k@30 Resource Utilization	4k@60 Resource Utilization	4k@120 Resource Utilization
LUTs	105k	2X105k	4X105k
Logic cells	180k	2X180k	4X180k
B-RAM	9Mbits	2X9Mbits	4X9Mbits
DSPs	340	2X340	4X340

Table-1 Logic resource utilization of 4k encoder at the frame rate of 30, 60, or 120

Logic Resources on Altera FPGAs:

The logic resources required on Altera FPGAs by the 4k@30/60/120 encoder IP core is listed in Table-2

Resources type	4k@30 Resource Utilization	4k@60 Resource Utilization	4k@120 Resource Utilization
ALM	60k	2X60k	4X60k
B-RAM	7Mbits	2X7Mbits	4X7Mbits
DSPs	310	2X310	4X310

Table-2 Logic resource utilization of 4k encoder at the frame rate of 30, 60, or 120

FPGA Examples:

The following Table-3 shows the FPGA examples for 4k@30, 4k@60, and 4k@120 resolutions. Other FPGAs are also supported, as long as the logic resources and clock speed meet the requirement.

Resolution@frame-rate	Xilinx FPGA Example	Altera FPGA Example
4k@30	Zynq-7 Z-7035	Arria-10 GX220
4k@60	Zynq-7 Z-7045	Arria-10 GX480
4k@120	Kintex Ultrascale XCKU060	Arria-10 GX660

Table-3 Examples for Xilinx and Altera FPGAs

5. H.264 4k Video Encoder Integration Sheet

When the encoder is delivered in IP core format, it is a ready-to-use "netlist" core for FPGAs. Fig. 2 shows the inputs and outputs of the encoder core.

The H.264 4k video encoder IP core integration details are provided in a separate document under the title of "H.264 4k Video Encoder IP Core Integration Sheet".

Fig. 2 The inputs and outputs of the H.264 video encoder IP Core

6. The H.264 4k Encoder Module

SOC supplies the H.264 4k encoder on a 2.7"x2.5" module (card), as shown in Fig. 3. The module provide complete function of 4k video/audio encoding. The module connects to the host product/PCB via a device-to-PCB connector, as shown in Fig. 4.

Refer to the Product Brief and Datasheet of SOC MPEG Codec Modules for technical details.

Fig. 3 SOC MPEG Codec Module

Fig. 4. Device-to-PCB connectors

7. The H.264 4k Encoder Chipset

SOC Technologies provides a series of CODEC chipsets, the SOC-Mcodec family, which can be dropped onto user PCBs as ASIC video encoders and decoders. The SOC-Mcodec family of chipsets support all MPEG standards, including H.264, H.265, and MPEG-2, and all industrial standard resolutions, including SD, 720, 1080, 4K, and 8K, with frame rates of up to 120 fps.

The SOC H.264 4k Encoder Chipset includes an FPGA and FLASH preconfigured with SOC's H.264 4k Encoder IP Core. It is an ASIC that receives raw video/audio and outputs an H.264 video stream with optional AAC/MP2/MP3 audio compression. It supports resolutions up 4k at 120 fps.

Fig. 5 SOC-Mcodec chipsets

SOC CODEC Chipsets are fully pre-configured FPGA chips that are designed to function just like traditional ASIC chipsets, integrated onto user PCB by connecting the pins.

The Chipset I/O interfaces can be customized to virtually any customer specifications, making them the most flexible CODEC chipsets on the market. This is especially useful if your system demands non-standard I/O interfaces - let us tailor the interfaces to work in harmony with your system.

Unlike traditional ASICs, SOC's CODEC chipset firmware may be updated to change its functionality or I/O interfaces if needed.

The SOC CODEC Chipsets are built using SOC Technologies' portfolio of ultra-high-performance CODEC and peripheral IP Cores. You can expect high quality, high speed, low latency, and low power-consumption.

With high volume productions of FPGAs, today's FPGAs are fabricated using the most current silicon technologies that are used for computer CPUs, such as the new 10nm silicon class. This makes the FPGA based ASICs away ahead of the traditional MPEG codec ASICs, especially in power consumption, speed, and cost.

8. Related Documents

1. Integration Sheet – Encoder IP Cores
2. API Manual – H.264 Encoder IP Core
3. Pin Assignment Sheet – Encoder Modules
4. Pin Assignment Sheet – Encoder Chipsets

9. User API

The encoder (IP core or module) is controllable through a user API, which allows the user to control the operations of the encoder through setting the control registers at runtime. Refer to the "H.264 Video/Audio Encoder API Manual" for details.

10. Technical Support

SOC provides technical support for all its products, which include documentation, e-mail based, and telephone based support. Additional support services, such as on-site training services, can be subscribed from SOC as a service contract.

11. IP core upgrading

Upgrade is usually a part of the technical support contract signed individually. Upgrade programs are available for subscription after the technical support period. On-line automatic upgrading can also be arranged if desirable.

12. Related Information

The SOC H.264 4k video decoders are implemented based on the same technology of this H.264 4k video encoder. Refer to the datasheets of SOC H.264 4k video decoders for details.

13. Ordering Information

The SOC H.264 4k video/audio encoder IP cores are available for licensing, or one-time fee purchase, or a combination of one-time fee plus reduced royalty payments. The module can be order on a unit by unit basis.

Please contact SOC sales by telephone +1 519 880-8609 or e-mail: sales@soctechnologies.com

14. Document Revisions

Version #	Revision Date	Notes
V.1.0	2014/02/15	First release
V.1.1	2014/08/10	
V.2.0	2015/03/15	Major revision
V.2.1	2016/05/15	