SOC MPEG-2 Video/Audio Decoder IP Core Datasheet

System-On-Chip (SOC) Technologies

1. Product Overview

The SOC MPEG-2 video decoder is a single chip solution that supports single or multi-stream MPEG-2 video decoding for all industrial standard resolutions including QVGA, SD and HD up to 1080p/60fps.

The SOC MPEG-2 video decoder is implemented based on SOC's proprietary single-clock driven all-hardware technology (without microprocessors or embedded software), which has significant advantages of high-speed (low latency), small footprint (low power), high video quality, and high resolution capability. The decoder fits into a small footprint FPGA, for example, the low-end Xilinx Spartan-6 series, such as the XC6SLX45.

The SOC MPEG-2 video decoder decodes both 4:2:0 and 4:2:2 streams with automatic selection. The decoder is suited for both consumer products and high-end applications, such as broadcast, satellite video transmissions, digital cinema, and medical devices. It is also well suited for smart cell phones and mobile devices, as it has low power consumption.

The SOC decoder series can be integrated with an audio decoder to provide an all-in-one decoding solution. SOC also integrates network modules, TCP/UDP-IP, Ethernet MACs, as well as the MPEG transport de-multiplexer into the design to produce full system-on-chip systems. Customized versions of these products are available on request.

2. The SOC MPEG-2 Video Decoder Architecture

Fig. 1 is the block diagram of the SOC MPEG-2 video decoder. It is a self-contained FPGA IP core that can be either placed into a single FPGA or integrated with other logic blocks in the same FPGA for system-on-chip solutions.

All of the blocks in the design, shown in Fig. 1, are implemented in hardware without embedded processors or embedded software, which offers high speed, low logic resource consumption, and low power. Input to the decoder is standard MPEG-2 elementary stream without bit rate limitation. The output of the decoder is the video stream for standard display devices with frames properly ordered. SOC also provides an MPEG transport decoder to allow the input to the decoder to be in the form of MPEG transport streams.

The decoder also automatically detects missing data, if any, and compensates for the missing blocks using the corresponding blocks in the neighboring frames to increase the overall video quality.

The SOC MPEG-2 video decoder requires two external clock sources with one at 100MHz and the second at 27MHz. The decoder also requires an external DDR3 memory of minimum of 256MB for 1080p resolution.

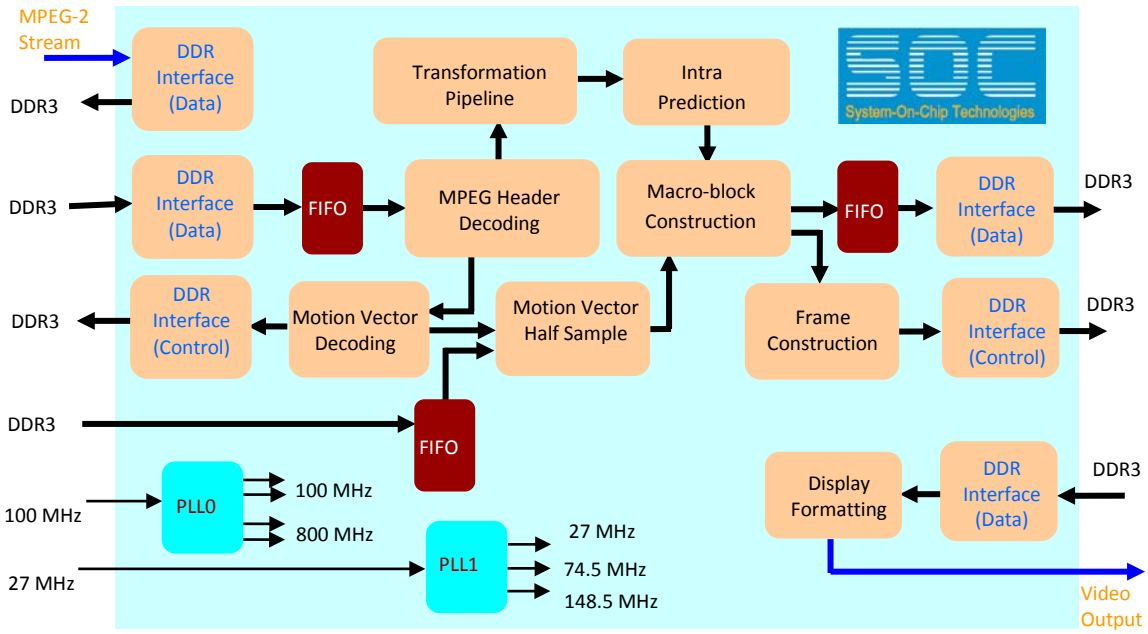

Fig. 1 Block Diagram of SOC MPEG-2 video decoder

3. Technical Specifications

Chroma Format:

The SOC MPEG-2 video decoder supports both:

- 4:2:0
- 4:2:2.

Input Data Rate:

There is no limitation on the data rate of the input, as long as MPEG-2 compliant.

Latency:

The SOC MPEG-2 video decoder has very low latency (<0.25ms) due to its hardware implementation.

A summary of these specifications is provided in Table-1.

Table-1 Specification Summary Table

FEATURE	DESCRIPTION
MPEG Profile	High
MPEG Level	Up to High
Resolution	QVGA, SD, and HD up to 1080p @30 or 60fps (4k resolution available under a separate product release)
Input bit rate	There is no bit rate limitation
Latency	<0.25ms
Power	< 700mw
Interlace Stream	Support
FPGA size	Spartan-6 LX45 single channel for1080p
Multiple channels	Available (larger FPGA chip)
Integrated Audio decoder	Available
MPEG Transport DeMux	Available
Ethernet MAC	Available for integration
UDP/TCP-IP	Available for integration
User defined I/O	Supported
Copy to ASIC	Supported

4. Targeted FPGAs and Logic Resources

The SOC MPEG-2 video decoder supports most of the FPAGs, including:

- Xilinx Spartan-6 FPGAs
- Xilinx Virtex-6 FPGAs
- Xilinx Virtex-5 FPGAs
- Xilinx Kyntex-7 FPGAs
- Xilinx Artix-7 FPGAs
- Altera Stratic IV and V
- Altera Arria V
- Altera Arria 10
- Altera Cyclone V

Logic Resources on Xilinx FPGAs:

The logic resources required on Xilinx FPGAs by the MPEG-2 decoder IP core is listed in Table-1

Resources type	Resource Utilization
LUTs	12k
Logic cells	21k
B-RAM	1Mbits
DSPs	54

Table-1 Logic resource utilization of the MPEG-2 decoder for up to 60fps

Logic Resources on Altera FPGAs:

The logic resources required on Altera FPGAs by the HMPEG-2 encoder IP core is listed in Table-2

Resources type	Resource Utilization
ALM	9k
B-RAM	1Mbits
DSPs	54

Table-2 Logic resource utilization of the MPEG-2 decoder for up to 60fps

FPGA Examples:

The following Table-3 shows the FPGA examples for 1080p@30, 1080p@60 resolutions. Other FPGAs are also supported, as long as the logic resources and clock speed meet the requirement.

Resolution@frame-rate	Xilinx FPGA Example	Altera FPGA Example
1080p@30	Spartan-6 LX45	Cyclone-5 5CEA2
1080p@60	Artix-7 XC7A50T	Arria-10 GX160

Table-3 Examples for Xilinx and Altera FPGAs

5. Applications

- TV set-top Boxes
- IPTVs
- Video conferencing devices
- Consumer products
- Smart cell phones
- Satellite video/audio transmission equipment
- Digital cinemas
- Broadcast Equipment
- Medical imaging devices
- Others

The SOC MPEG-2 video decoder is designed for high-performance, but it can also be used for low-end application, such as video surveillance products. SOC provides customizations for these products.

6. Use the SOC MPEG-2 Video Decoder (Product Format)

SOC provides three packaging formats to customers, which allows for ease-of-use of the product. These formats include:

1. FPGA IP core
   – A self-contained IP core for FPGA users.

2. Video/audio decoder modules
   – A small circuit board that integrates all required components for both video and audio decoding.

3. Customized system-on-chip solutions surrounding the decoder
   – SOC provides integration with other IP cores to produce a system-on-chip solution.

Technical data for using the above four formats are further elaborated in the following sections.

7. The MPEG-2 Video Decoder IP Core Integration Sheet

When the decoder is delivered in IP core format, it is a ready-to-use "netlist" core for FPGAs. Fig. 2 shows the input and output of the decoder core.

The MPEG-2 video decoder IP core integration details are provided in a separate document under the title of "MPEG-2 Video Decoder IP Core Integration Sheet".

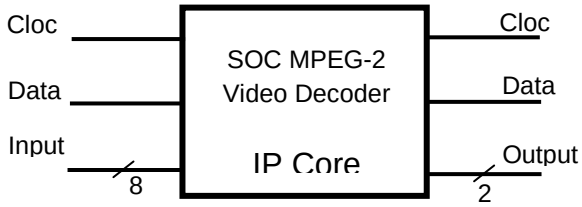

Fig. 2 The input and output of the MPEG-2 IP Core

8. The SOC MPEG Codec Modules

SOC supplies the MPEG2 decoder on a 2.7"x1.7" module (card), as shown in Fig. 3. The modules provide complete function of video/audio decoding. The module connects to the host product/PCB via a device-to-PCB connector, as shown in Fig. 4.

Fig. 3. SOC H.264 Decoder Module

Fig. 4. Device-to-PCB connectors

The SOC MPEG Codec Modules can be directly connected to I/O interface chips for product fabrication, as shown in Fig. 5, or connected to an FPGA or a Microcontroller for user system integrations, as shown in Fig. 6.

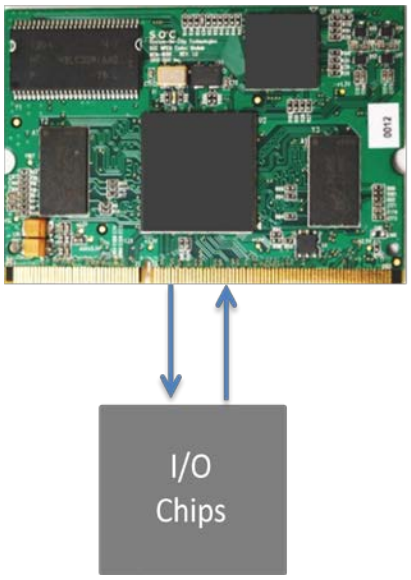

Fig. 5 SOC MPEG Codec Module directly connects to I/O interfaces in user product

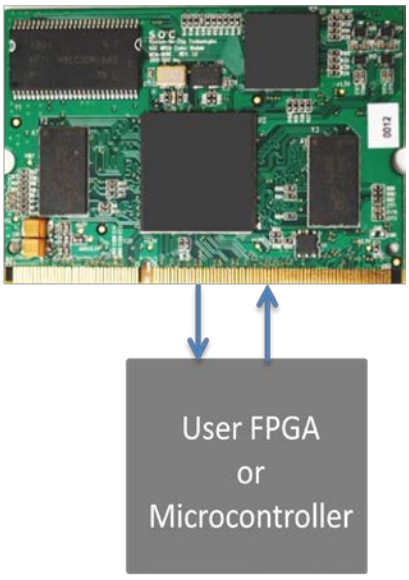

Fig. 6 SOC MPEG Codec Module connects to FPGA/microcontroller for user integration

Refer to the Product Brief and Datasheet of SOC MPEG Codec Modules for technical details.

9. The MPEG-2 HD Decoder Chipset

SOC Technologies provides a series of CODEC chipsets, the SOC-Mcodec family, which can be dropped onto user PCBs as ASIC video encoders and decoders. The SOC-Mcodec family of chipsets support all MPEG standards, including H.264, H.265, and MPEG-2, and all industrial standard resolutions, including SD, 720, 1080, 4K, and 8K, with frame rates of up to 120 fps.

The SOC MPEG-2 HD Decoder Chipset includes an FPGA and FLASH preconfigured with SOC's MPEG-2 HD Encoder IP Core. It is an ASIC that receives raw video/audio and outputs an H.264 video stream with optional AAC/MP2/MP3 audio compression. It supports resolutions up HD at 60 fps.

Fig. 5 SOC-Mcodec chipsets

SOC CODEC Chipsets are fully pre-configured FPGA chips that are designed to function just like traditional ASIC chipsets, integrated onto user PCB by connecting the pins.

The Chipset I/O interfaces can be customized to virtually any customer specifications, making them the most flexible CODEC chipsets on the market. This is especially useful if your system demands non-standard I/O interfaces - let us tailor the interfaces to work in harmony with your system.

Unlike traditional ASICs, SOC's CODEC chipset firmware may be updated to change its functionality or I/O interfaces if needed.

The SOC CODEC Chipsets are built using SOC Technologies' portfolio of ultra-high-performance CODEC and peripheral IP Cores. You can expect high quality, high speed, low latency, and low power-consumption.

With high volume productions of FPGAs, today's FPGAs are fabricated using the most current silicon technologies that are used for computer CPUs, such as the new 10nm silicon class. This makes the FPGA based ASICs away ahead of the traditional MPEG codec ASICs, especially in power consumption, speed, and cost.

10. Customized Solutions Surrounding the MPEG-2 Decoder

SOC also provides customized system-on-chip integrations based on the MPEG-2 video/audio decoders. Fig. 7 shows an example of an integrated decoder solution for HD video over the Internet with HDMI output.

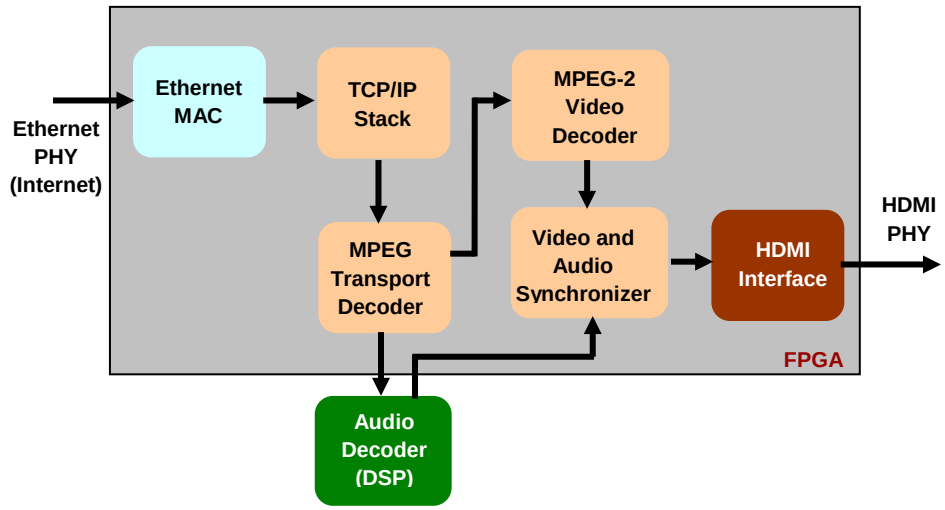

Fig. 7 Example system-on-chip solution: HD-over-IP decoder

11. MPEG-2 and H.264 Multi-protocol Decoder

SOC also offers a combined (multi-protocol) MPEG-2 and H.264 video decoder, as shown in Fig. 8, to allow the decoder to decode either MPEG-2 or H.264 automatically according to the input stream. All the packaging formats discussed in Section 6 are available for the multi-

protocol decoder. This multi-protocol MPEG video decoder can also be configured to decode both MPEG-2 and H.264 streams con-currently.

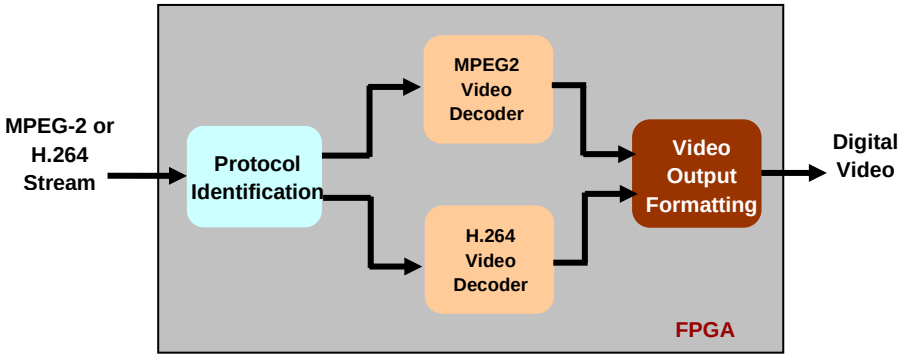

Fig. 8 Multi-protocol video decoder

Fig. 9 shows the block diagram of the multi-protocol video and audio decoder. One FPGA and one DSP are used in the system to achieve high-performance and low cost. Similar to the video only decoder shown in Fig. 8, the video/audio decoder can also be configured to decode two MPEG transport streams with one being the MPEG-2 and the other being the H.264.

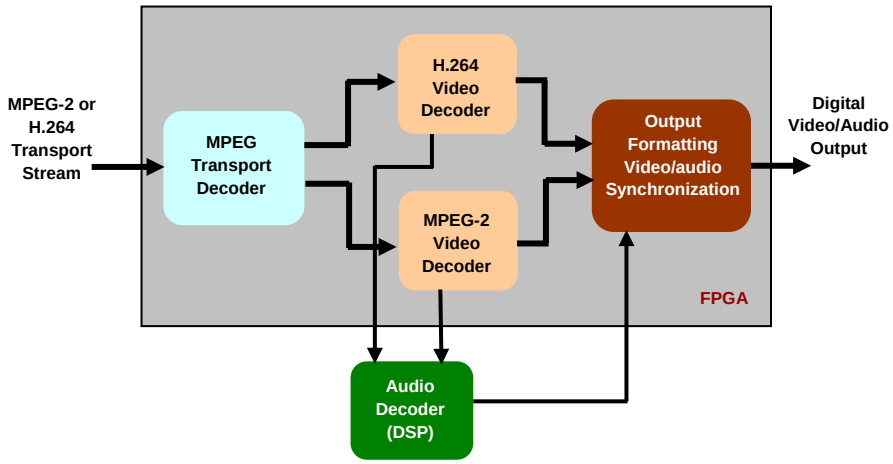

Fig. 9 Multi-protocol video/audio decoder

12. Technical Support

SOC provides technical support for all its products, which include documentation, web site based, and telephone based support. Additional support services, such as on-site training services, can be subscribed from SOC as a service contract.

13. IP core Upgrading

Upgrades to the IP core are available to all the delivery formats discussed in Section 6. Upgrade is usually a part of the technical support contract signed individually. On-line automatic upgrading can also be arranged if desirable.

14. Related Information

SOC has launched the H.264 video decoder, based on the same technology of its MPEG-2 video decoder. The only difference between the MPEG-2 and the H.264 decoders is the MPEG standard, while the H.264 decoder is MPEG-4 part-10 AVC, i.e. H.264, compliant, this MPEG-2 decoder is MPEG-2 compliant. The datasheet of SOC H.264 video decoder resembles this datasheet in many ways, as the two decoders are similar in terms of architecture and functionality, except for the standards.

15. Related Documents

1. Integration Sheet – Decoder IP Cores
2. API Manual – mpeg-2 Decoder IP Core
3. Pin Assignment Sheet – Decoder Modules
4. Pin Assignment Sheet – Decoder Chipsets

16. Ordering Information

The SOC MPEG-2 video/audio decoder IP cores are available for licensing, or one-time fee purchase, or a combination of one-time fee plus reduced royalty payments. The FPGA driver

format of the MPEG-2 decoder is designed for customers who want to purchase the driver chips without licensing contracts. The driver chip is sold at a competitive price on a chip by chip basis. The SOC MPEG-2 video/audio decoder unit is a complete solution for video and audio decoding at low cost. It is sold on unit by unit basis without limitation on the quantities. It can also be licensed in IP core format, to allow the user to integrate other IP cores into the products.
SOC also provides integration of the MPEG-2 and/or H.264 decoders with other functional IP cores of SOC or customer provided IP cores. A combination of NRE and licensing royalties is normally considered, which is negotiated on case by case basis.

Please contact SOC sales by telephone +1 519 880-8609 or e-mail: sales@soctechnologies.com

17. Document Revisions

Version #	Revision Date	Notes
V.1.0	2008/02/15	First release
V.1.1	2009/05/10	
V.2.0	2010/08/15	Major revision
V.2.1	2011/05/15	
V.3.0	2012/11/15	Major revision
V.3.1	2013/08/10	
V.4.0	2014/03/15	Major revision
V.4.1	2015/11/10	
V.5.0	2016/05/18	Major revision