System-On-Chip Technologies

Specification Sheet

MPEG-2 Video Encoder IP Core

Product Description

SOC provides the MPEG-2 encoder in three formats: IP core for FPGAs, ASIC Chipset, and a standalone all-in-one modules.

IP cores are available for both Xilinx and Intel (Altera) FPGAs. SOC configures the cores according to user specifications, including I/O formats.

The SOC codec chipsets are AISC chips based on the SOC IP cores. Standard MPEG-2 encoder chipsets for different specifications are available.

The SOC codec modules are System-on-Module (SoM) small circuit boards, based on the SOC codec IP cores, that can be connected to user devices/PCBs using a standard DDR3 memory connector.

Users have the options of using one of these product formats, based on the applications.

SOC also offers product development kits, which allow users to develop products using the SOC MPEG-2 video/audio encoder IP cores, chipsets, or modules.

Key Features

- All-hardware design (no embedded software)
- High Speed (Low latency)
- Small Silicon Footprint
- Low Power
- High Reliability (due to hardware architecture)
- High-Video Quality
- Low Output Bandwidth
- High-Output Bandwidth Version Available
- User controllable API
- Option of IP Core or Module
- Video Transmission (Network) Cores available
- Development Board available

IP Core Specifications

- Standard: MPEG-2/H.262 (ISO/IEC 13818)
- Profiles: High, Main, Baseline
- Output bit rates: 1-100Mbps & above
- Video resolutions: Up to 1080i/p
- Frame rate: Up to 60fps
- Chroma formats: 4:2:2 or 4:2:0
- Output format: MPEG-2 Elementary, or Transport Stream
- Video input format: RGB or YUV
- Audio support: MPEG-2 Layer-II or AAC
- Latency: 0.25ms
- Power consumption: 0.8w (IP core)
- FPGAs: Xilinx or Intel (Altera)

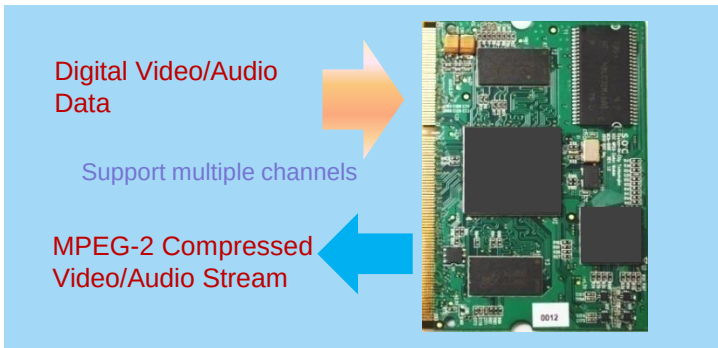
FPGA Resources

	Xilinx FPGAs	Intel FPGAs
Logic Resources:	50,000 LUTs	30,000 ALMs
Block RAMs:	1.6Mb	1.5Mb
DSPs:	200 DSPs	210 DSPs

MPEG-2 Video/Audio Encoder Chipset

SOC-MCodec™

MPEG-2 Video/Audio Encoder Module



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