SOC H.264-to-MPEG2 Video/Audio Transcoder IP Core Datasheet

System-On-Chip (SOC) Technologies

1. Key Features

1. Profile&Level: H.264 High profile (up to 4.2L)
2. Chroma Format: 4:2:0 or 4:2:2
3. Frame Rate: up to 60fps
4. Resolution: SD (STSC and Pal), 720i, 720p, 1080i, and 1080p
5. Input Stream: Transport or Elementary
6. Latency: 0.5ms
7. Minimum FPGA: Xilinx Artix-7 or Altera Cyclone-V
8. Multiple streams: 2 Streams on Xilinx Kintex-7 K325

2. Product Overview

The SOC H.264-to-MPEG2 video/audio transcoder is a single chip solution that supports single or multi-stream H.264-to-MPEG2 transcoding for all industrial standard resolutions including QVGA, SD and HD up to 1080p/60fps.

SOC provides the versions of the H.264-to-MPEG2 video/audio transcoder IP core for FPGAs of Xilinx, and Altera. SOC also supplies all-in-one encoder modules based on the same H.264-to-MPEG2 transcoder IP core. Refer to the Product Brief and Datasheet for SOC MPEG codec modules for details.

The SOC H.264-to-MPEG2 video/audio transcoder is implemented based on SOC's high-speed H.264 video/audio decoder and MPEG-2 video/audio encoder. The transcoder decodes the input H.264 stream into video/audio data and re-encodes the video/audio data into an MPEG-2 stream in either elementary (video only) or transport stream format. This mechanism provides the best accuracy for transcoding H.264 streams to MPEG-2 streams. Furthermore, the SOC H.264 video decoder and the MPEG-2 video encoder are implemented based on the SOC proprietary single-clock driven all-hardware technology (without microprocessors or embedded software), which has significant advantages of high-speed (low latency), small footprint (low power), high video quality, and high resolution.

The SOC transcoder can be integrated with network modules, TCP/UDP-IP and Ethernet, to produce a full system-on-chip transcoder system. Customized versions of these products are available on request.

3. The SOC H.264-to-MPEG2 Transcoder Architecture

Fig. 1 shows the architecture of the SOC H.264-to-MPEG2 video/audio transcoder. It fully decodes the input H.264 stream and re-encodes it into an MPEG-2 stream. The MPEG transport stream DeMux and Mux module are included to allow the transcoder to transcode either elementary or transport streams. The transcoder is a self-contained FPGA IP core that can be either placed into a single FPGA or integrated with other logic blocks in the same FPGA for system-on-chip solutions.

All of the modules related to the video, shown in Fig. 1, are implemented in hardware without embedded processors or embedded software, which offers high speed, low logic resource consumption, and low power. Input to the transcoder is standard H.264 elementary or transport stream without bit rate limitation. The output of the transcoder is MPEG-2 stream in either elementary (video only) or transport stream. A user interface is provided to allow the user to control the H.264 encoder to produce desired output stream.

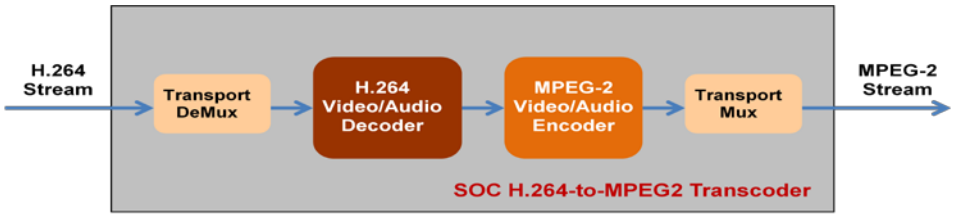

Fig. 1 Block Diagram of SOC H.264-to-MPEG2 video/audio transcoder

4. Technical Specifications

Please refer to the Datasheets of H.264 decoder and MPEG-2 encoder for technical specifications.

5. Targeted FPGAs and Logic Resources

The SOC H.264-to-MPEG2 transcoder fits into most of the Xilinx and Altera FPGAs, such as:

- Spartan-6
- Virtex-6
- Kintex-7
- Virtex-7
- Artix-7
- Cyclone-V
- Arria-V
- Stratix-IV, V

The logic resources required by the transcoder equals to the combined logic required of by the H.264 decoder plus the MPEG-2 encoder, which are:

Logic Resources on Xilinx FPGAs:

The logic resources required on Xilinx FPGAs by the H.264-to-MPEG2 transcoder IP core is listed in Table-1

Resources type	Resource Utilization
LUTs	150k
Logic cells	250k
B-RAM	10Mbits
DSPs	350

Table-1 Logic resource utilization of the H.264-to-MPEG2 transcoder for up to 60fps

Logic Resources on Altera FPGAs:

The logic resources required on Altera FPGAs by the H.264-to-MPEG2 transcoder IP core is listed in Table-2

Resources type	Resource Utilization
ALM	120k
B-RAM	8Mbits
DSPs	350

Table-2 Logic resource utilization of the MPEG2-to-H.264 transcoder for up to 60fps

6. Using the SOC H.264-to-MPEG2 Video/Audio Transcoder

SOC provides three packaging formats to customers, which allows for easy-of-use of the product. These formats include:

1. FPGA IP core
   – A self-contained IP core for FPGA users, in either bit file or encrypted netlist.

2. SOC MPEG Codec Modules
   – SOC provide all its codecs, including the H.264-to-MPEG2 transcoder, on small circuit boards that integrate all required components for video or audio or both video and audio encoding/decoding/transcoding. The codec module connects to a host device via a standard DDR3 connector. SOC also provides evaluation/development boards for both modules and IP cores.

3. Customized system-on-chip solutions surrounding the transcoder
   – SOC provides integration with other IP cores to produce a system-on-chip solution.

Technical data for using the above three formats are described in the following Sections.

7. H.264-to-MPEG2 Transcoder IP Core Integration Sheet

When the transcoder is delivered in IP core format, it is a ready-to-use "netlist" core for FPGAs. SOC supports both Xilinx and Altera FPGAs.

The H.264-to-MPEG2 transcoder IP core integration details are provided in a separate document under the title of "H.264-to-MPEG2 Video Encoder IP Core Integration Sheet".

8. SOC H.264-to-MPEG2 Transcoder Modules

SOC supplies the H.264-to-MPEG2 transcoder on a 2.7"x2.0" module (card), as shown in Fig. 5. The modules provide complete function of video/audio transcoding. The module connects to the host product/PCB via a DDR3 connector, as shown in Fig. 6.

Refer to the Product Brief and Datasheet of SOC MPEG Codec Modules for technical details.

Fig. 5 SOC MPEG Codec Module

Fig. 6. Device-to-PCB connectors

9. Customized Solutions Surrounding the H.264-to-MPEG2 Transcoder

SOC also provides customized system-on-chip integrations based on the H.264-to-MPEG2 video/audio trancoders. Contact SOC at sales@soctechnologies.com for details.

10. User API

The MPEG-2 encoder (IP core or module) is controllable through a user API, which allows the user to control the operations of the encoder through setting the control registers at runtime. Refer to the "MPEG-2 Video/Audio Encoder API Manual" for details.

11. Technical Support

SOC provides technical support for all its products, which include documentation, web site based, and telephone based support. Additional support services, such as on-site training services, can be subscribed from SOC as a service contract.

12. Ordering Information

The SOC MPEG-4/H.264 video/audio decoder IP cores are available for licensing or a combination of one-time fee plus reduced royalty payments.

The SOC H.264-to-MPEG2 trancoder modules are complete solution for video and audio transcoding at low cost. The modules are sold on a unit by unit basis without limitation on the quantities.

Please contact SOC sales by telephone +1 519 880-8609 or e-mail: sales@soctechnologies.com

13. Document Revisions

Version #	Revision Date	Notes
V.1.0	2012/02/15	First release
V.1.1	2013/05/10	
V.2.0	2014/08/15	Major revision
V.2.1	2015/05/15	
V.3.0	2016/11/15	Major revision