Super-low Latency RTP-UDP-IP Network Stack + Ethernet IP Core

System-On-Chip (SOC) Technologies

1. Product Overview

The SOC RTP-UDP-IP network stack IP core is an all-hardware implementation of the RTP (Real-time Transport Protocol), UDP (User Datagram Protocol), and IP (Internet Protocol) standards, which allow for FPGA-Internet communications. An Ethernet IP core normally comes with the RTP-UDP-IP core, which allows for direct connection to the IP networks via an Ethernet connection.

The SOC RTP-UDP-IP network stack + Ethernet combined IP core provides high speed (low latency of less than 5ms) operations, due to hardware implementation. It also requires a small amount of FPGA logic resources. It does not require any embedded processors or external memories.

The SOC "RTP-UDP-IP network stack + Ethernet" IP core supports Xilinx (Network stack for Altera FPGAs is a separate product release). Contact SOC sales for details: sales@soctechnologies.com

2. The SOC RTP-UDP-IP + Ethernet IP Core Architecture

Fig. 1 shows the architecture of the SOC "RTP-UDP-IP network stack + Ethernet" combined IP core. Users can choose UDP/IP or RTP/IP for their applications. All of the modules are implemented in FPGA logics, without embedded processors, which offers low latency, small silicon footprint, and low power consumption.

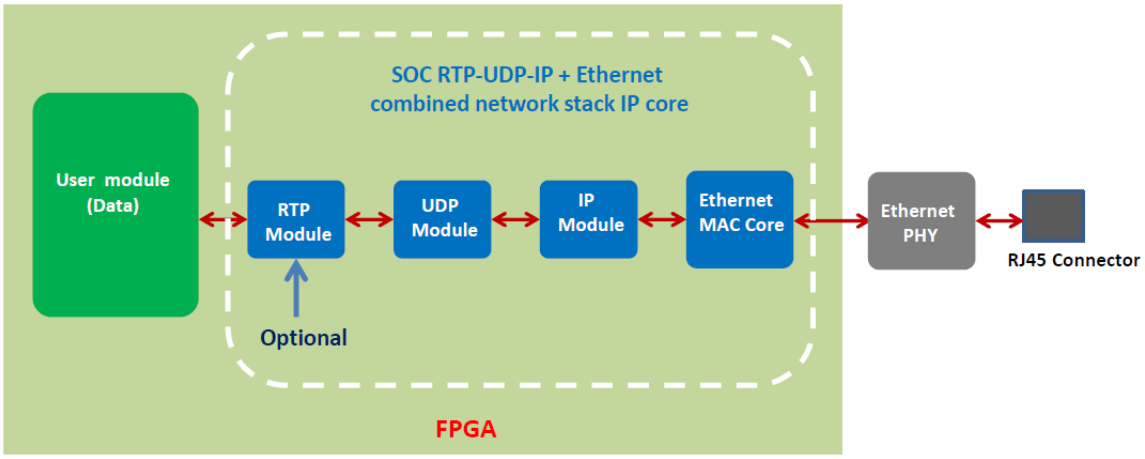

Fig. 1 The SOC RTP-UDP-IP network stack + Ethernet combined FPGA IP core

3. Technical Specifications

The SOC RTP-UDP-IP network stack + Ethernet combined FPGA IP core is fully compliant with the RTP, UPD, IP, and Ethernet standards:

RTP (Real-time Transport protocol) – RFC 3550

UDP (User Datagram Protocol) - RFC 768

IP (Internet Protocol) – IP V4

Ethernet – 10/100/1000BASE-T IEEE802.3 compliant.

FPGA resources: The FPGA resource utilization of the RTP-UDP-IP network stack + Ethernet combined IP core on the Xilinx Spart-6 LX150 FPGA:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	3121	184304	1%
Number of Slice LUTs	3492	92152	3%
Number of fully used LUT-FF pairs	795	5818	13%
Number of bonded IOBs	1	396	0%
Number of Block RAM/FIFO	12	268	4%
Number of BUFG/BUFGCTRLs	3	16	18%

Table-1: Logic resources: SOC RTP-UDP-IP network stack + Ethernet combined FPGA IP core on xc6slx150t-2fgg676

Latency: The overall latency of the RTP-UDP-IP network stack + Ethernet combined FPGA IP core is 5ms.

4. Targeted FPGAs

The SOC RTP-UDP-IP network stack + Ethernet combined FPGA IP core supports most of the Xilinx FPGAs, which include:

- Virtex-5
- Spartan-6
- Virtex-6
- Kitex-7
- Virtex-7
- Artix-7
- Zynq-7.

5. Integrating the SOC RTP-UDP-IP + Ethernet IP Core

Fig. 2 shows a diagram for integrating the network stack IP into a user design. User out going data are sent into the network IP core by 8 data lines, a clock, and a data enable. Data coming from the network are sent to the user via 8 data lines, a clock, and a data enable pin. A bi-directional connection to user API is also available which allows the user to change the configuration parameters, before or during running time.

A top level VHDL shell reference design is provided along with the IP core shipment. SOC also provides a reference PCB design as an example for connecting to the user FPGA and the Ethernet PHY.

SOC also licenses PCB schematics of evaluation boards, which is intended to reduce design time of user products. Contact SOC sales at sales@soctechnologies.com for details.

It should be noted that SOC licenses the Ethernet IP core (which is used inside the SOC network stack IP core, as shown in Fig. 1) from a third party. SOC can sell/license the network IP core with the Ethernet in bit file format. But, when the SOC network stack netlist is licensed by a SOC customer, an Ethernet IP core license from the Ethernet IP vendor is required. The customer will need to purchase the Ethernet IP core license from the vendor. Information for licensing the Ethernet IP core will be provided, along with the delivery of the SOC network netlist IP core.

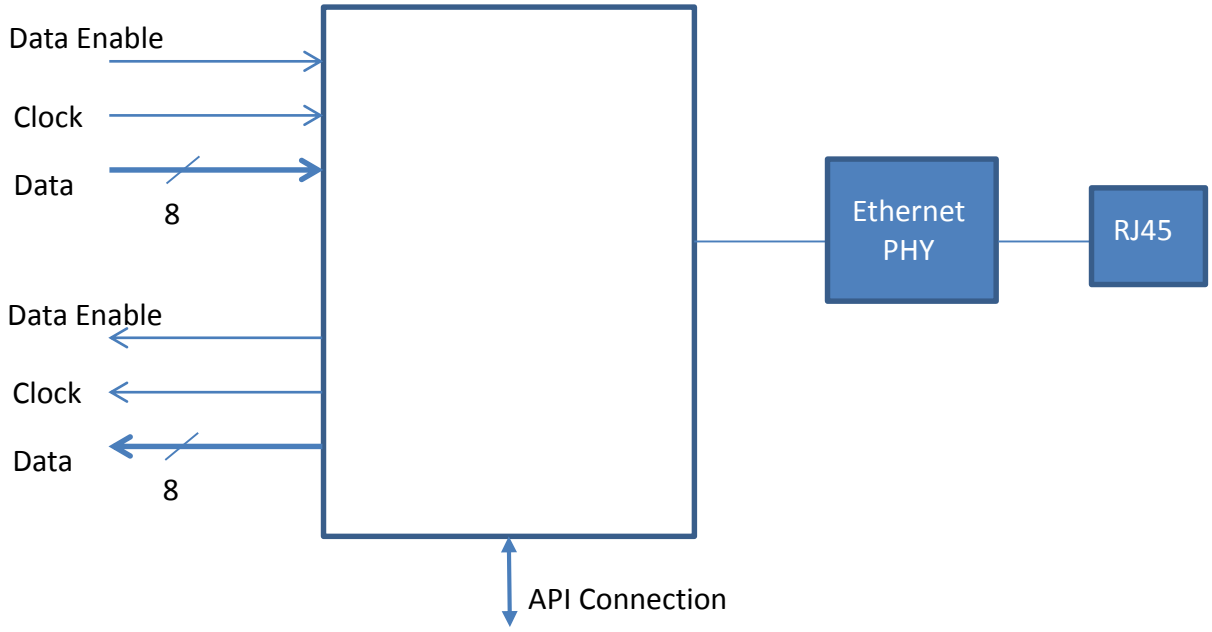

Fig. 2 Block diagram for integrating the SOC network stack IP into user designs